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PART - A

2 Marks Questions

Q.1

Sol. The traffic level for free electrons in conduction band will be always less than the traffic level for holes in valence band.

	μ_0	μ_h
Ge	$3800\text{cm}^2 / \text{v sec}$	$1800\text{cm}^2 / \text{v sec}$
Si	$1300\text{cm}^2 / \text{v sec}$	$500\text{cm}^2 / \text{v sec}$

Q.2

Sol. At OK

	Ge	Si	GaAs
E_g	0.785eV	1.21eV	1.58eV

As the energy gap between valence band and conduction band of GaAs is more than Ge and Si, so these are good semiconductor.

Q.3

Sol.

$$E_g = E_{g0} - \beta T$$

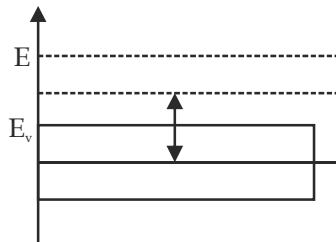
$$\begin{aligned}
 T = 27^\circ\text{C}, \quad [E_g(300\text{K})]_{\text{Si}} &= 1.21 - 3.6 \times 10^{-4} \times 300 \\
 &= 1.21 - (0.00108) \\
 &= 1.12\text{eV} \quad (1\text{eV} = 1.6 \times 10^{-19}\text{J}) \\
 [E_{g(300\text{K})}]_{\text{Ge}} &= 0.785 - 2.23 \times 10^{-4} \times 300 = 0.72\text{eV}
 \end{aligned}$$

Q.4

Sol. The fermi-level moves towards the C.B. in case of n-type and moves towards the V.B. in case of p-type.

Q.5

Sol.



$$E_{tp} = E_v + kT / n \left(\frac{N_v}{N_A} \right)$$

$$\text{if, } N_A > N_v \text{ then, } \ln \left(\frac{N_v}{N_A} \right) < 0$$

$$E_{tp} = E_v - (\text{Some value})$$

i.e. fermi level moves inside valence band.

Q.6

Sol. Conductivity, $(\sigma) = \frac{1}{\text{resistivity}}$

For a pure silicon, $\sigma = (\mu_n + \mu_p)n, e$

Where,

μ_n = electron mobility

μ_p = hole mobility

n_i = carrier concentration

e = electron charge = $1.6 \times 10^{-19} \text{C}$

Given that, $\mu_n = 3\mu_p$

So, $\frac{1}{3000} = (3\mu_p + \mu_p) \times 1.1 \times 10^6 \times 1.6 \times 10^{-19}$

or $\mu_p = 4.7348 \times 10^8 \text{ m}^2 / \text{V} - \text{sec}$

and $\mu_n = 3\mu_p = 3 \times 4.7348 \times 10^8 = 1.42 \times 10^9 \text{ m}^2 / \text{V} - \text{sec}$

Q.7 Prove that $n_i^2 = A_0 T^3 e^{-\frac{E_{go}}{kT}}$

Sol. $n.p = n_i^2$

$n_i^2 = N_C N_v e^{-\frac{(E_C - E_V)}{kT}}$

$\Rightarrow n_i^2 = A_0 T^3 e^{-\frac{(E_C - E_V)}{kT}}$ (as N_C and N_v are the function of temperature)

so, $\sigma_i \propto n_i T^{3/2}$

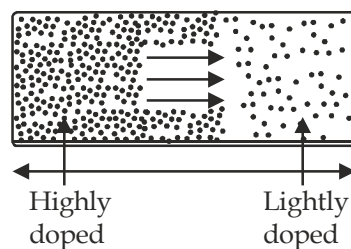
Q.8

Sol. Diffusion Current:

It occurs in a non-uniformly doped semiconductor,

- Rate of change of concentration with respect to distance x is called as diffusion current. It is also

called concentration gradient $\frac{dn}{dx}$



Non-uniformly doped semiconductor

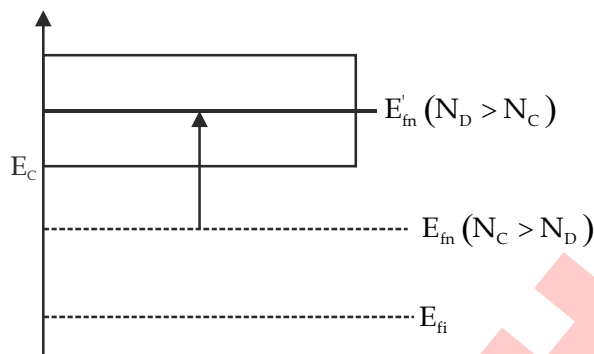
- Without electric field, there is movement of charge from high density to low density side, and this movement is called diffusion current.

i.e. $I_{\text{diff}} \neq 0$

- Best examples of non-uniformly doped SC will be P-N junction.

Q.9

Sol.



$$E_{fn} = E_c - kT \ln \frac{N_c}{N_D}$$

$$N_D > N_C \text{ then, } \ln \frac{N_c}{N_D} < 0$$

$$E_{fn} = E_c + (\text{some value})$$

i.e. fermi level moves inside the conduction band. e.g. tunnel diode.

Q.10

Sol. In case of n-type material or p-type material the fermi level moves towards the intrinsic fermi level.

Q.11

Sol. Acceptor density, $N_a = 10^{18} \text{ cm}^{-3}$
 Donor density, $N_d = 10^{15} \text{ cm}^{-3}$
 Intrinsic concentration, $N_i = 1.5 \times 10^{10} \text{ cm}^{-3}$

Built-in voltage, $V_i = V_T \ln \frac{N_a N_d}{N_i^2}$

where $V_T = \frac{kT}{q}$

$$\therefore V_i = \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} \ln \frac{10^{18} \times 10^{15}}{(1.5 \times 10^{10})^2} = 0.75 \text{ V}$$

Q.12

Sol.

$$C_j \propto V_j^{-1/2}$$

$$\frac{C_{j_2}}{C_{j_1}} = \sqrt{\frac{V_1}{V_2}} = \sqrt{\frac{1}{4}} = \frac{1}{2}$$

$$C_{j_2} = \frac{C_{j_1}}{2} = \frac{1 \text{ pF}}{2} = 0.5 \text{ pF}$$

Q.13

Sol.

$$I_D = K(V_{GS} - V_T)^2$$

$$1\text{mA} = K(900 - 400)^2$$

$$K = \frac{1\text{mA} / V^2}{10^4 \times 25}$$

When,

$$V_{GS} = 1400, I_D = K(V_{GS} - V_T)^2$$

$$= \frac{1\text{mA}}{25 \times 10^4 V^2} (1400 - 400)^2 \times V^2 = \frac{1\text{mA} \times 100}{25 \times 10^4} \times 10^4$$

$$I_D = 4\text{mA}$$

Q.14

Sol.

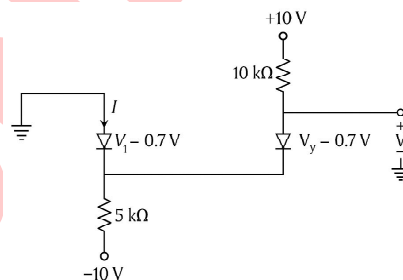
Advantages:

1. MOSFET transconductance increase with drain current, the consequence is less distortion.
2. MOSFET consumes less power than BJT.
3. MOSFET's input impedance are very high so they do not load the circuits. Loading effect does not arise.
4. In MOSFET greater bandwidth.
5. In MOSFET thermal stability is more compared than BJT.
6. Effect of noise is less than BJT. So high signal to noise ratio.
7. MOSFET are small compare to BJT's so it fabricated easily and space saving scheme on the IC's.

Disadvantages:

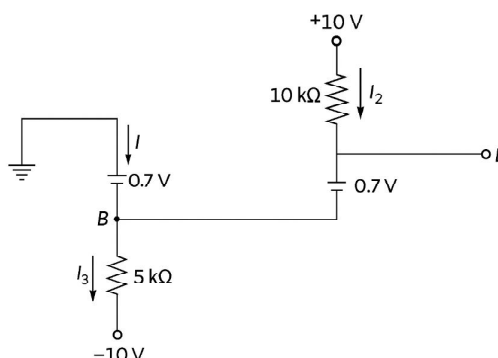
1. The transconductance in MOSFET is low (gain low), i.e., bandwidth is less.
2. MOSFET is very sensitive to electrostatic charge so it may be destroy when you touch the pins of a MOSFET devices by hand.
3. MOSFET is more costlier than BJT.
4. Gain bandwidth product is lower than BJT.

Q.15 Find I and V for the circuit shown below:



Sol.

We shall assume that D_1 and D_2 are forward bias then the equivalent circuit can be redrawn as shown below: So, voltage at node B is



$$V_B = -0.7V$$

and

$$\begin{aligned} V &= 0.7 + V_B \\ &= 0.7 - 0.7 = 0V \end{aligned}$$

Hence, I_2 can be calculated as

$$I_2 = \frac{10 - 0}{10k} = 1mA$$

For I_3 current

$$I_3 = \frac{10 - 0.7}{5} = 1.86 \text{ mA}$$

Now applying KCL at node B

$$\begin{aligned} I &= I_3 - I_2 \\ &= 1.86mA - 1mA \end{aligned}$$

$\Rightarrow$

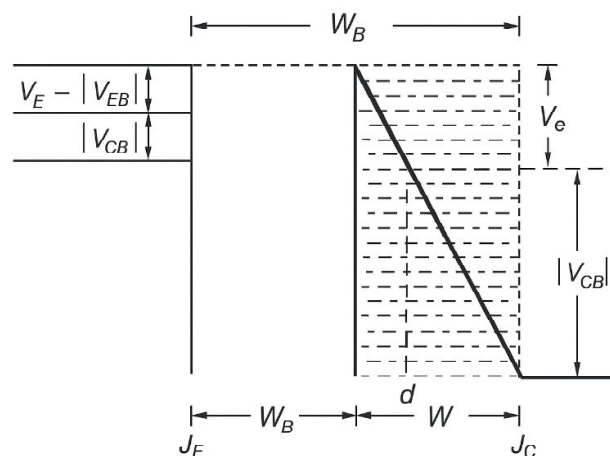
$$I = 0.86mA$$

Thus D_1 is conducting as originally assumed and the final result is $I = 0.86 \text{ mA}$ and $V = 0V$.

Q.16

Sol. Early Effect :

When BJT is biased in active region the emitter junction (J_E) is forward-biased but the collector junction is reverse biased, then in Fig. the barrier width at J_E is negligible as compared to space-charge width W at J_C .

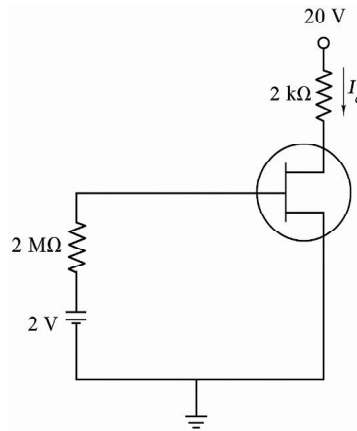


The transition region at junction is a region of uncovered charges on both sides of junction at positions occupied by impurity atoms. As the voltage applied across the junction increases, transition region penetrates deeper into collector and base. As neutrality of charges must be maintained, so the number

of uncovered charges on each side remains equal. Since the doping in base is substantially smaller than that of collector, the penetration of the transition region into the base is much larger than that in collector. Hence the collector depletion region is neglected in Fig., and all immobile charges are indicated in base region.

If metallurgical base width is W_B , then the effective electrical base width is $W'_B = W_B - W$. This modulation of effective base width by collector voltage is known as the Early effect or Base width modulation.

Q.17 I_D and V_{DS} under DC conditions are respectively



Sol. DC condition :

$$V_{GS} = -2V$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$= 10 \left[1 - \left(\frac{-2}{-8} \right) \right]^2 = 5.625 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 20 - 5.625 \text{ mA} \times 2 \text{ k}\Omega$$

$$= 8.75 \text{ V}$$

PART - B

5 Marks Questions

Q.18

Sol. The Mass-action Law :

In a semiconductor under thermal equilibrium (constant temperature) the product of electrons and holes concentrations is always a constant and is equal to the square of intrinsic carrier concentration.

$$np = n_i^2$$

The intrinsic concentration n_i is a function of temperature.

The law is mainly used to calculate the concentration of minority carriers. In n-type semiconductor, the electrons are called the majority carriers, and the holes are called the minority carriers. In a p-type material, the holes are the majority carriers, and the electrons are the minority carriers.

For a p-type semiconductor,
$$p_n = \frac{n_i^2}{n_n}$$



For an n-type semiconductor, $n_n = \frac{n_i}{p_n}$

or, Minority carrier concentration = $\frac{n_i^2}{\text{Majority carrier concentration}}$

but, Majority carrier concentration $\propto$ Doping concentration

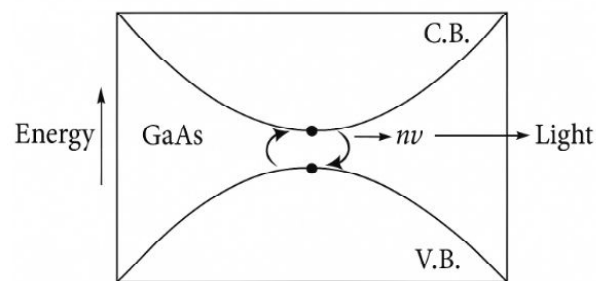
so, Minority carrier concentration $\propto \frac{1}{\text{Doping concentration}}$

or, $\boxed{\text{Minority carrier concentration} \times \text{Doping concentration} = n_i^2}$

In a semiconductor, if majority carrier concentration increases the minority carrier concentration decreases this is due to the recombinations.

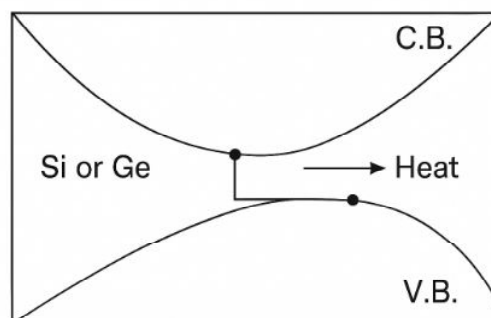
Q.19

Sol. Direct band gap:



- (i) During recombination electron will fall from C.B. to V.B. releasing same optical energy.
- (ii) The momentum of highest energy level of V.B. and lowest energy level of C.B. are same.
- (iii) Direct band gap types are GaAs, GaP etc. these all are used for light generation.
- (iv) Carrier life time is less.

Indirect band gap:



- (i) During recombination when the electron is falling from C.B. to V.B. it releases heat energy.
- (ii) Momentum level is not same.
- (iii) Si and Ge
- (iv) Carrier life time is more.

NOTE: Movement of electron from Conduction band (C.B.) to Valence band (V.B.) into the holes is called recombination.

Q.20

Sol. It is the minimum forward voltage required so that the forward current flows through the diode. Cut-in voltage is also known as:

- Offset voltage
- Threshold voltage
- Knee voltage
- Break voltage

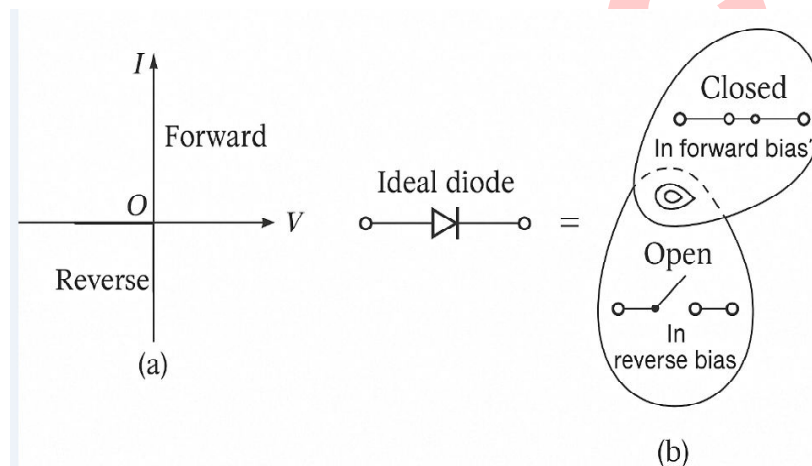
For Ge diode $V_\gamma = 0.1\text{V} - 0.5\text{V}$; Typical value 0.2 V

For Si diode $V_\gamma = 0.6\text{V} - 0.9\text{V}$; Typical value 0.7 V

Cut-in voltage decreases with temperature. For 1°C rise in temperature, it is reduced by 2.5 mV.

Q.21

Sol. The Ideal Diode



We have seen that a diode permits only unidirectional conduction. It conducts well in the forward direction and poorly in the reverse direction. It would have been ideal if a diode acted as a perfect conductor (with zero voltage across it) when forward-biased, and as a perfect insulator (with no current through it) when reverse-biased. The V-I characteristics of such an ideal diode would be as shown in Figure (a). An ideal diode acts like an automatic switch. When the current tries to flow in the forward direction, the switch is closed. On the other hand, when the current tries to flow the other way (against the direction of the diode arrow) the switch is open.

Q.22

Sol. **Avalanche Breakdown**

A thermally generated carrier (part of the reverse saturation current) falls down the junction barrier and acquires energy from the applied potential. This carrier collides with a crystal ion and imparts sufficient energy to disrupt a covalent bond. In addition to the original carrier, a new electron-hole pair has now been generated. Thus each new carrier may in turn, produce additional carriers through collision and the action of disrupting bonds. This cumulative process is referred to as avalanche multiplication. It results in large reverse currents, and the diode is said to be in the region of avalanche breakdown. Breakdown voltages are greater than 6 V. Avalanche breakdown voltages increase with temperature.

Zener Breakdown

It is possible to initiate breakdown through a direct rupture of the bonds. Because of the existence of the electric field at the junction, a sufficiently strong force may be exerted on a bound electron by the field to tear it out of its covalent bond. The new hole-electron pair which is created increases the

reverse current. Note that this process, called zener breakdown, does not involve collisions of carriers with the crystal ions (as does avalanche multiplication).

It is found that zener breakdown occurs at a field of approximately 2×10^7 V/m. This value is reached at voltages below about 6 V for heavily doped diodes. For lightly doped diodes the breakdown voltage is higher, and avalanche multiplication is the predominant effect.

Zener breakdown voltage decreases with the temperature.

Q.23

Sol. FET Vs BJT

BJT is a current-controlled device while FET is a voltage controlled device. BJT is a bipolar device while FET is unipolar device. Input impedance of FET is at a level of 1 to several hundred megaohms. It far exceeds the typical input resistance levels of the BJT transistor configurations - a very important characteristic in the design of linear ac amplifier systems.

BJTs have much higher sensitivity to changes in the applied signal. In general, FETs are more temperature stable than BJTs and they are also usually smaller in construction than BJTs, making them particularly suitable for IC chips. Voltage gain of FET is low so that FET has lower value of gain-BW product. Hence its operation is limited to relatively lower frequencies compared to that of the BJT amplifier.

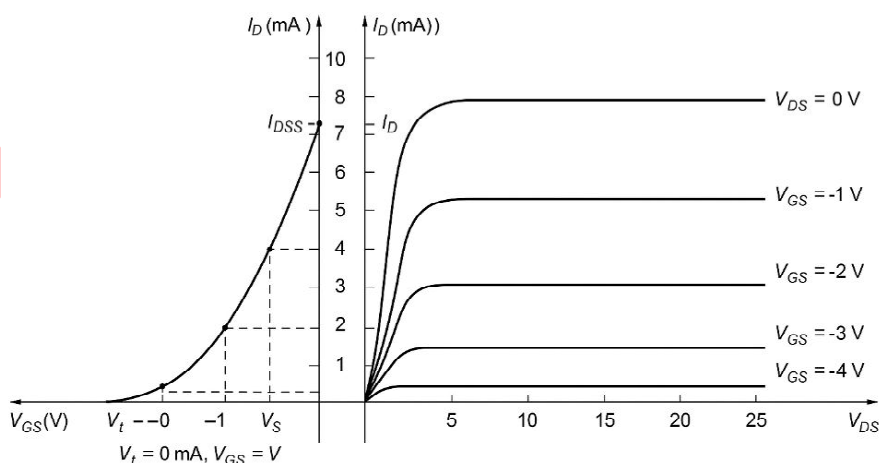
BJT is faster than FET. The power dissipation of FET is less than that of BJT. Area (space) required by the FET on the chip is less than BJT.

FET is more used in digital circuits Due to no offset voltage FET is better chopper than BJT. FET is less noisy than BJT FET has higher input impedance than BJT, FET is a unipolar device. The current flow in FET is due to majority carriers as there are no minority carriers.

Q.24

Sol. In amplifier applications the FET is almost always used in the region beyond pinch-off (also called the constant-current pentode, or current-saturation region). Let the saturation drain current be designated by, and send its value with the gate shorted to the source ($V_{GS} = 0$) by I_{DSS} it has found that the transfer characteristic, giving the relationship between I_{DS} and V_{GS} can be approximated by the parabola

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$



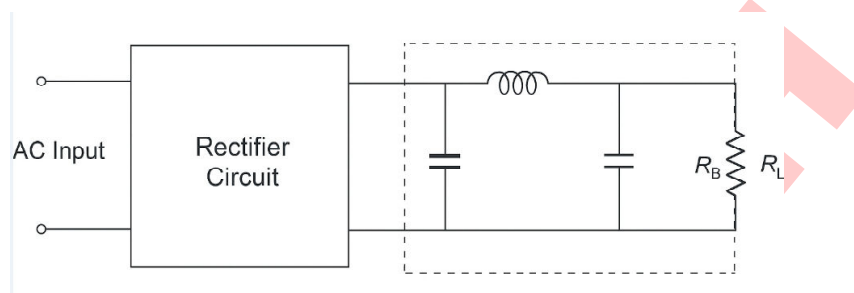
The transfer characteristics defined by Shockley's equation (3.7) are unaffected by the network in which the device is employed. In FET drain current is drift current since it is controlled by electric field intensity produced in the channel.



Q.25

Sol. Bleeder Resistor

It is used in high voltage dc supplies to provide discharge path for capacitor when R_L is not present. In absence of bleeder resistor a large dc voltage will be present across capacitor even when the ac supply is turned-off. This high dc voltage across capacitor can cause electric shock if someone touches the plate of capacitor. Bleeder resistor is also used in LC filter so that the inductor current can bleed (or flow) through bleeder resistance R_B if R_L is not present. With the help of following figure where bleeder resistance R_B is used in CLC filter we will try to summarize the purpose of bleeder resistor in filter circuits.



Here

- The value of bleeder resistance should be such that it draws only 10% of total load current.
- It provides better voltage regulation.
- It provides safety to operator by providing discharge path to the capacitor.
- Single power supply can be used to provide more voltage.
- Bleeder resistance can be used as voltage divider for tapping out any desired output.

Q.26

Sol.

$$I_{ZK} = 25 \times 10^{-3} \text{ A}$$

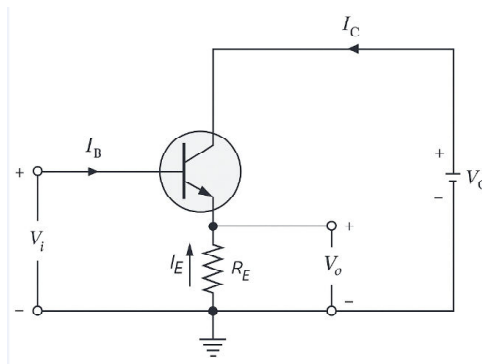
$$I_L = \frac{10}{100} = 0.1 \text{ A}$$

$$I_s = I_L + I_{ZK}$$

$$= 100 + 25 = 125 \text{ mA}$$

$$R = \frac{20 - 10}{125 \times 10^{-3}} = 80 \Omega$$

Q.27

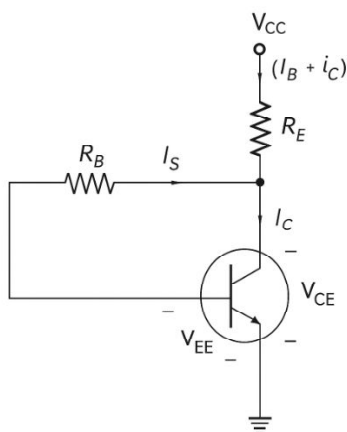
Sol. The Common-Collector Configuration:

Another transistor configuration, shown in Fig., is known as the Common-Collector (CC) configuration. The circuit is basically the same as the circuit of Fig., with the exception that the load resistor is in emitter circuit rather than in collector circuit. If we continue to specify the operation of circuit in terms of the currents which flow, the operation for common-collector is much same as for common-emitter configuration. When base current is I_{CO} the emitter current will be zero, and no current will flow in load. As the transistor is brought out of this back-biased condition by increasing the magnitude of the base current, the transistor will pass through the active region and eventually reach saturation. In this condition whole supply voltages, except for a very small drop across the transistor, will appear across the load..

Q.28

Sol. **Collector to Base Bias Circuit:**

An improvement in bias stability is obtained if tapping for bias is taken from the collector terminal instead of from the collector supply point as shown in Fig.



Applying KVL in input loop, we have

$$-V_{CC} + (I_B + I_C)R_C + I_B R_B + V_{BE} = 0 \quad \dots(i)$$

Using $I_C \approx \beta I_B$ we have

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{\left(1 + \frac{1}{\beta}\right)R_C + R_B} \quad \dots(ii)$$

Now applying KVL in the output loop, we have

$$\Rightarrow -V_{CC} + R_C(I_B + I_C) + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - R_C(I_B + I_C) \quad \dots(iii)$$

With the help of equations (ii) and (iii) we can calculate operating point for given biasing circuit.

Stability Factor:

To calculate stability factor, differentiating equation (i) with respect to I_C , we have

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_B + R_C}$$

Putting above value in equation, we have

$$S = \frac{\beta + 1}{1 + \beta \frac{R_C}{R_B + R_C}}$$



Advantage:

- Here stability factor is smaller than $(\beta + 1)$, hence an improvement in stability is obtained over fixed bias circuit.

Disadvantage:

- Stability factor depends upon R_C . If R_C becomes smaller or zero then stability factor becomes very large and I_C does not remain stable.
- Resistance R_B connected from collector to base causes negative feedback due which voltage gain of the amplifier circuit decreases.

Q.29

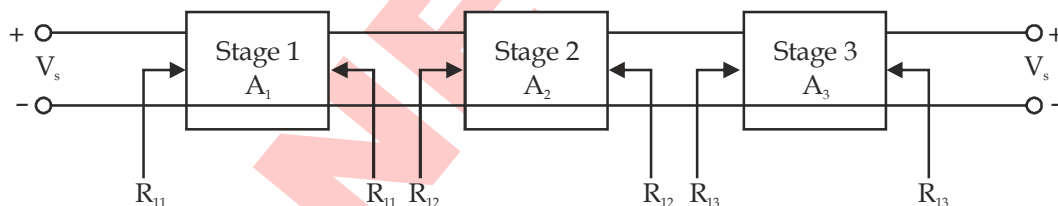
Sol. Thermal Runaway:

The maximum average power $P_{D(max)}$ which a transistor can dissipate depends upon the transistor consideration and may lie in the range from a few milliwatts to 200 W. The maximum power is limited by the temperature that collector-to-base junction can withstand. The junction temperature may rise either due to rise in ambient temperature or due to self-heating. The maximum power dissipation is usually specified for transistor enclosure (case) of ambient temperature of 25°C. The problem of self-heating results from the power dissipated at collector junction. As a consequence of junction power dissipation, the junction temperature rises, and this in turn increases the collector current, with a subsequent increase in power dissipation. If this phenomenon, referred to thermal runaway, continues, it may result in permanent damage to the transistor.

Q.30

Sol. Multistage Amplifiers:

Transistor amplifier circuits can be connected in series, or cascaded, as shown in Fig. (4.25). This may be done either to increase an overall small-signal voltage gain or to provide an overall voltage gain greater than 1, with very low output resistance. The overall voltage or current gain, in general, is not simply the product of the individual amplification factor. For example, the gain of stage 1 is a function of the input resistance of stage 2. In other words, loading effects may have to be taken into account



There are many possible multistage configurations; we will examine some of them here, in order to understand the type of analysis required.

Q.31

Sol. Common Mode Rejection Ratio :

The ability of a differential amplifier to reject a common-mode signal is described in terms of the Common Mode Rejection Ratio (CMRR). The CMRR is a figure of merit for the diff-amp and is defined as

$$CMRR = \left| \frac{A_d}{A_{cm}} \right|$$

For an ideal differential-amplifier, $A_{cm} = 0$ and $CMRR = \infty$. Usually, the CMRR is expressed in decibels, as follows:

$$CMRR_{dB} = 20 \log_{10} \left| \frac{A_d}{A_{cm}} \right|$$

In practice, it is advantageous to use a differential amplifier with higher CMRR since this amplifier is better able to reject common-mode signals.



Q.32

Sol. Sampling Network :

Two sampling blocks are shown in figure. In figure (a) the output voltage is sampled by connecting the feedback network in shunt across the output. This type of connection is referred to as voltage or node sampling.

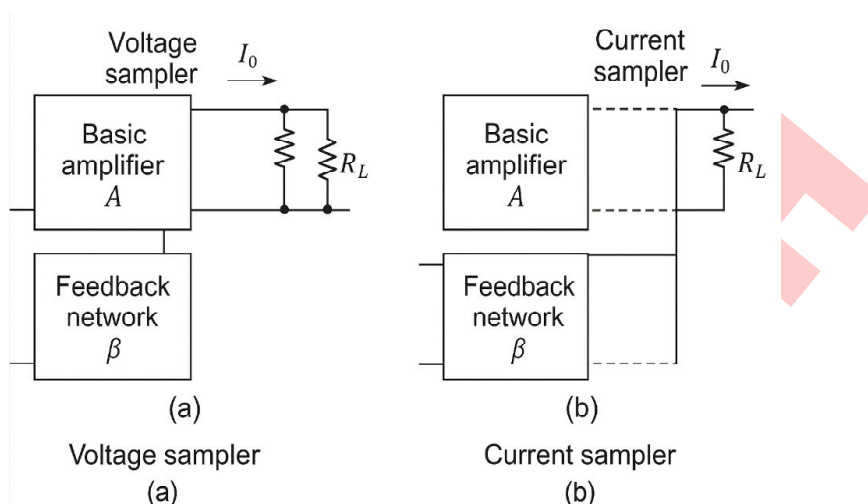


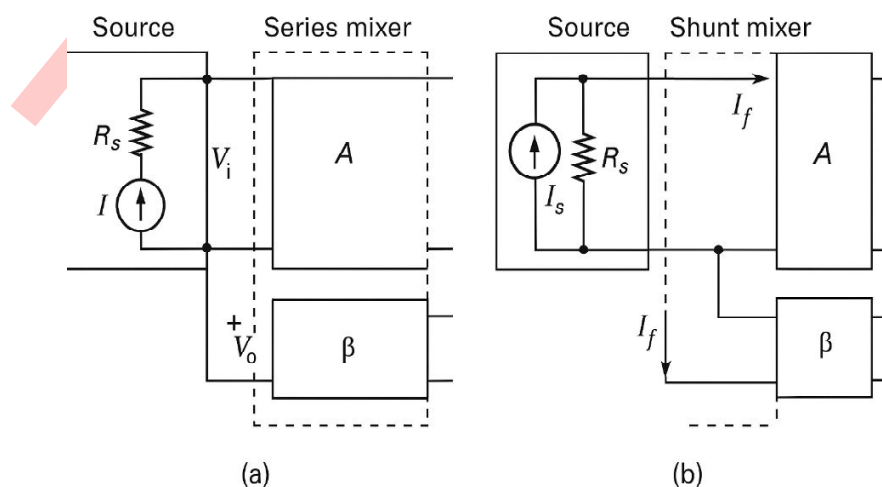
Figure:- Feedback connections at the output of a basic amplifier, sampling the output (a) voltage and (b) current

Another feedback connection which samples the output current is shown in figure (b), where the feedback network is connected in series with the output. This type of connection is referred to as current or loop sampling. Other sampling networks are also possible.

Q.33

Sol. Comparator or Mixer Network :

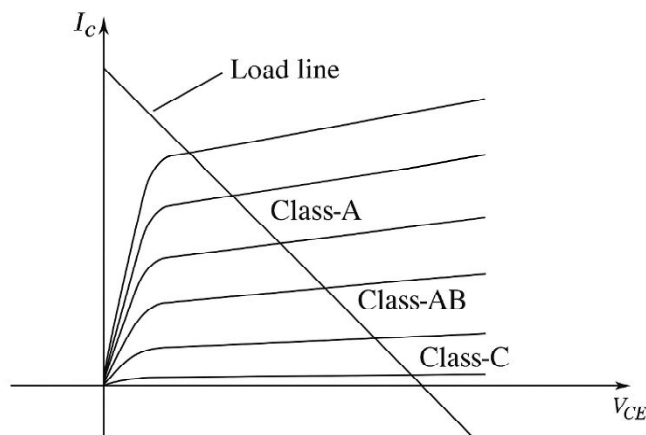
Two mixing blocks are shown in figure, (figure (a) and (b)] shows a simple and very common series (loop) input and shunt (node) input connections respectively. A differential amplifier is often used as a mixer. Such an amplifier has two inputs and gives an output proportional to the difference between the signals at two inputs.



Q.34

Sol. **Class-A Amplifier :**

An amplifier in which operating point is located approximately at the centre of the load line is known as class-A amplifier.



Advantage: It produces least distortion in the output among all power amplifiers.

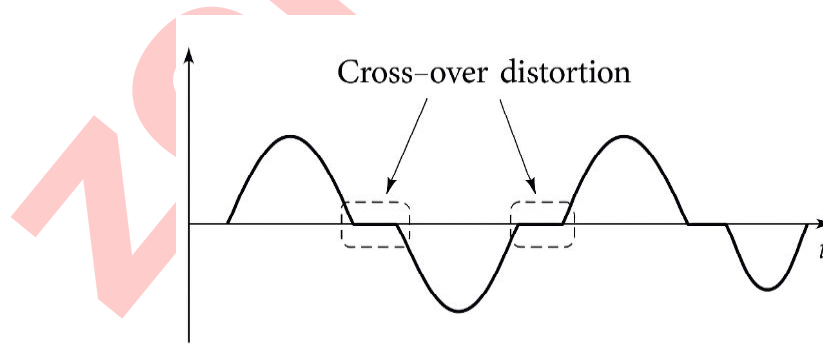
Drawback: In this power amplifier quiescent power dissipation is very large which means transistor dissipates higher power when AC input is not applied.

Application: Class-A amplifier is used as voltage amplifier. It is not preferred as power amplifier due to greater quiescent power dissipation.

Q.35

Sol. **Cross-Over Distortion :**

Practically a transistor can begin conduction only if base to emitter voltage is greater than $V_{BE \text{ cut-in}}$. Therefore, when one transistor turns off the other transistor can not begin conduction immediately, hence both transistors remain off for a short duration due to which output current becomes zero. So, the shape of output current waveform does not remain sinusoidal. It becomes distorted as shown in Fig. Hence, distortion occurs in the output and this distortion is known as cross-over distortion.



Q.36

Sol. **Slew Rate :**

Slew rate (SR) is defined as the maximum rate of change in output voltage per unit of time and is expressed in volts per microseconds. In equation form,

$$SR = \left. \frac{dV_0}{dt} \right|_{\text{maximum}} \quad \text{V} / \mu\text{s}$$

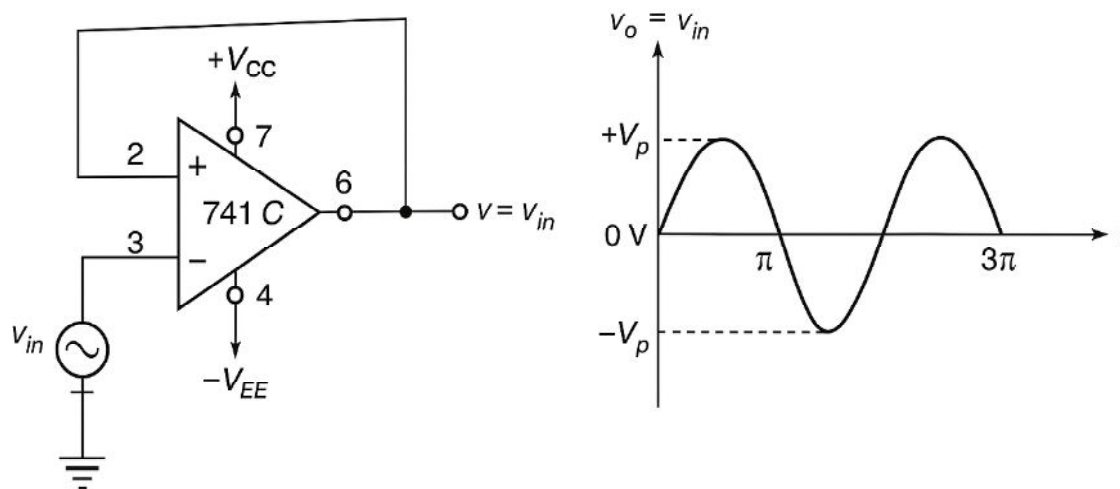


Note:-

- Slew rate indicates how rapidly the output of an op-amp can change in response to change in the input frequency.
- The slew rate of an op-amp is fixed; therefore, if the slope requirements of the output signal are greater than slew rate, then distortion occurs.

Slew Rate Equation :

Since the slew rate on a data sheet is generally listed for a unity gain, let us consider a voltage follower shown in figure. Furthermore, let us assume that the input is a large-amplitude and high-frequency sine wave.



The equation for the sine wave is

$$v_{in} = V_m \sin \omega t$$

or

$$v_o = V_m \sin \omega t$$

The rate of change of the output is

$$\frac{dv_o}{dt} = v_m \omega \cos \omega t$$

and the maximum rate of change of output occurs when $\cos \omega t = 1$. That is,

$$\left. \frac{dv_o}{dt} \right|_{\max} = V_m \omega$$

or

$$SR = 2\pi f V_m \text{ V} / \mu\text{sec}$$

$\Rightarrow$

$$SR = \frac{2\pi f V_m}{10^6} \text{ V} / \mu\text{sec}$$

where,

SR = slew rate V / (μsec)

f = input frequency (Hz)

V_m = peak value of the output sine wave (volts).

Q.37

Sol. **Characteristics of Ideal Op-Amp :**

An ideal Op-amp would exhibit the following electrical characteristics:

- Infinite voltage gain A .
 - Infinite input resistance R_i so that almost any signal source can drive it and there is no loading of the preceding stage.
 - Zero output resistance R_o so that output can drive an infinite number of other devices.
 - Zero output voltage when input voltage is zero.
 - Infinite bandwidth so that any frequency signal from 0 to ∞ Hz can be amplified without any attenuation.
 - Infinite common-mode rejection ratio so that the output common-mode noise voltage is zero.
- Infinite slew rate so that output voltage changes simultaneously with input voltage changes. There are practical op-amps that can be made to approximate some of these characteristics using a negative feedback arrangement. In particular, the input resistance, output resistance and bandwidth can be brought close to ideal values by this method.

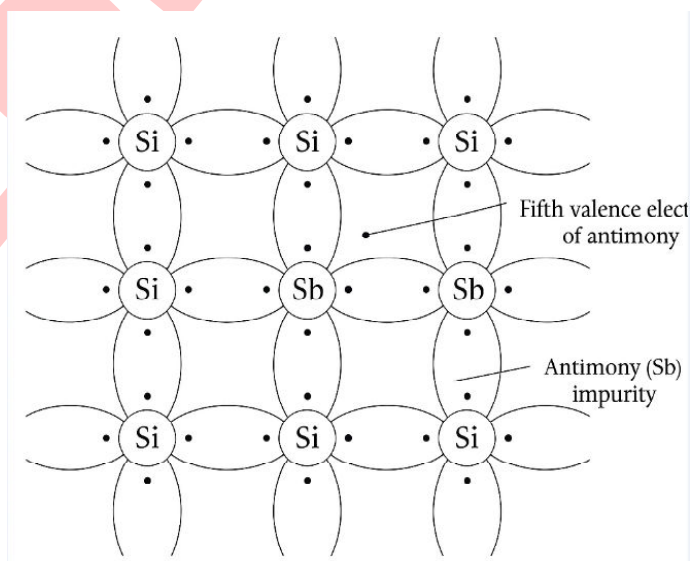
PART - C

20 Marks Questions

Q.38

Sol. **n-type semiconductor**

An n-type semiconductor is created by introducing impurity elements that have five valence electrons (pentavalent), such as antimony, arsenic and phosphorus. The effect of such impurity elements is indicated in figure. Note that the four covalent bonds are still present. There is, however an additional fifth electron due to the impurity atom, which is unassociated with any particular covalent bond. This remaining electron loosely bound to its parent atom (antimony) atom, is relatively free to move within the newly formed n-type material. Since the inserted impurity atom has donated a relatively "free" electron to the structure:



Diffused impurities with five valence electrons are called donor atoms.

When impurities or lattice defects are introduced into an otherwise perfect crystal, additional levels are created in the energy band structure, usually within the band gap. For example, an impurity from column V of the periodic table (P, As and Sb) introduces an energy level very near the conduction band in Ge or Si. Such an impurity level is called a donor level. In case of germanium, the distance of new discrete allowable energy level is only 0.01 eV (0.05 eV in silicon) below the conduction band, and therefore at room temperature almost all the "fifth" electrons of the donor material are raised into the conduction band.

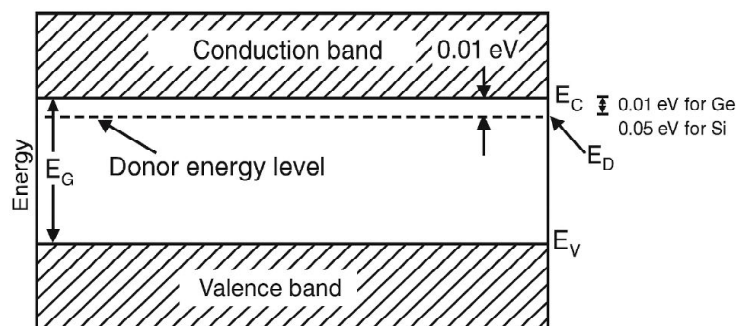
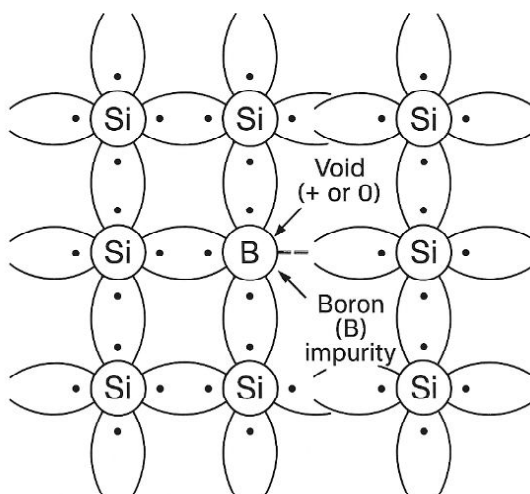


Figure-1.6: Energy-band diagram of *n*-type semiconductor

NOTE :- *n*-type material is as a whole electrically neutral since ideally the number of positively charged protons in the nuclei is still equal to the number of free and orbiting negatively charged electrons in the structure.

p-type semiconductor :

The *p*-type semiconductor is formed by doping a pure germanium or silicon crystal with impurity atoms having three valence electrons. The elements most frequently used for this purpose are boron, gallium and indium.

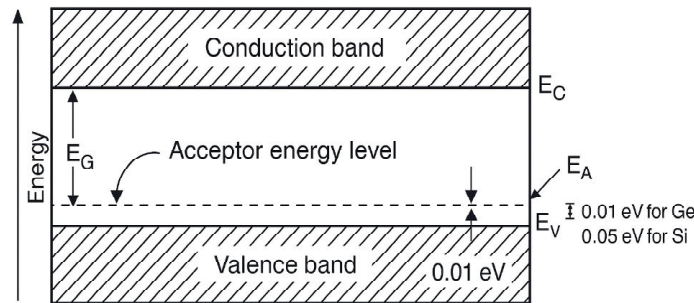


Note that, there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a hole and is represented by a small circle or a plus sign, indicating the absence of a negative charge. Since the resulting vacancy will readily accept a free electron;



The diffused impurities with three valence electrons are called acceptor atoms:

The resulting p-type material is electrically neutral for the same reasons described for the n-type material. Atoms from Column-III (B, Al, Ga and In) introduce impurity levels in Ge or Si near the valence band. These levels are empty of electrons at OK. At low temperatures, enough thermal energy is available to excite electrons from the valence band into the impurity level, leaving behind holes in the valence band. Since this type of impurity level "accepts" electrons from the valence band, it is called an acceptor level.



Q.39

Sol. **Reverse-bias condition ($V_D < 0$ V):**

If an external potential is applied across the p-n-junction such that the positive terminal is connected to the n-type material and negative terminal is connected to the p-type material as shown in Figure. The number of uncovered ions will increase due to the large number of free electrons/holes drawn to the respective potential of the applied voltage. The net effect, therefore, is a widening of the depletion region. As a result majority carriers can not cross the barrier, effectively reducing the majority current flow to zero. The number of minority carriers however, entering the depletion region will not change, resulting in minority-carrier flow across the junction.

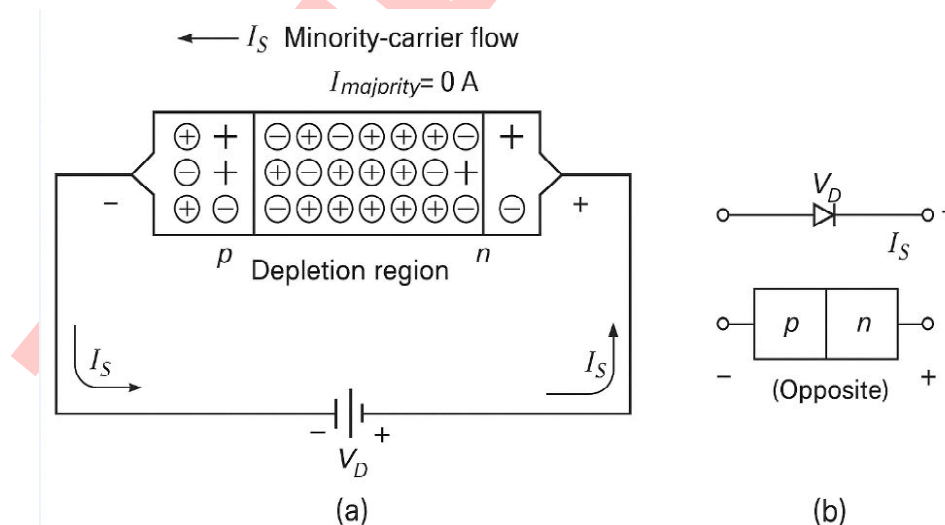


Figure:- Reverse-biased p-njunction (a) Internal distribution of charge under reverse-bias condition (b) Reverse-bias polarity and direction of reverse saturation current

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_s or I_0 .

Also called as minority carrier current or leakage current or thermally generated current. If leakage current is small, the device will have very good thermal stability. It is highly sensitive to temperature.

It doubles for every 10°C rise in temperature for both Si and Ge.

$$I_{s(T_2)} = I_{s(T_1)} 2^{\left(\frac{T_2 - T_1}{10}\right)} \text{ A}$$

$\Rightarrow$ Leakage current for $\begin{matrix} \text{Ge Diode : } \mu\text{A} \\ \text{Si Diode : } \text{nA} \end{matrix}$

The greatest advantage of Si is smaller leakage currents.

Expression for Diode Current

The general characteristics of a semiconductor diode can be defined by Schokley's equation, for the forward-and reverse bias regions

$$I_D = I_s (e^{V_D / \eta V_T} - 1)$$

where I_s is the reverse saturation current; V_D is the applied forward bias voltage across the junction. η is an ideality factor, which is a function of the operating conditions and physical construction

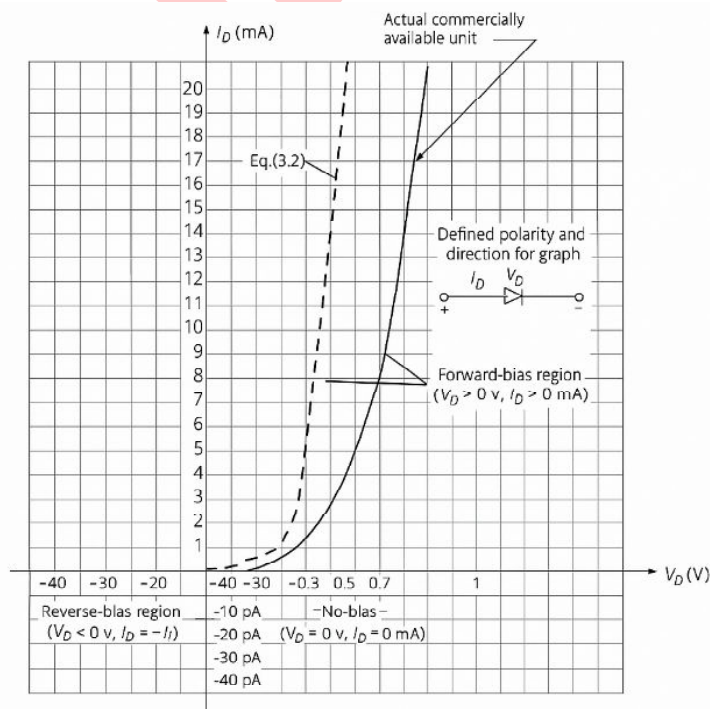
$\begin{matrix} \text{for Ge } \eta = 1 \\ \text{for Si } \eta = 2 \end{matrix}$. η also called as recombination factor.

V_T is the thermal voltage.

For positive values of V_D ; $I_D = I_s e^{V_D / \eta V_T}$ (V_D positive) ... (2.3)

For negative values of V_D ; $I_D \cong -I_s$ (V_D negative) ... (2.4)

with the help of above equations we can draw the characteristics of a semiconductor diode which is shown in Figure.



Q.40

Sol. Half-wave Rectifier- The basic circuit for half-wave rectification is shown in Fig. (a). We can assume that the diode has essentially infinite resistance in the reverse direction (for a voltage v less than the cut-in voltage V_γ) and a small and constant resistance R_f in the forward direction (for $v > V_\gamma$). Since in a rectifier circuit the input $v_i = V_m \sin \omega t$ has a peak value V_m which is very large compared with the offset voltage V_γ , we assume in the following discussion that $V_\gamma = 0$. Subject to this idealization of the diode characteristic, the current i in the diode or load R_L is given by

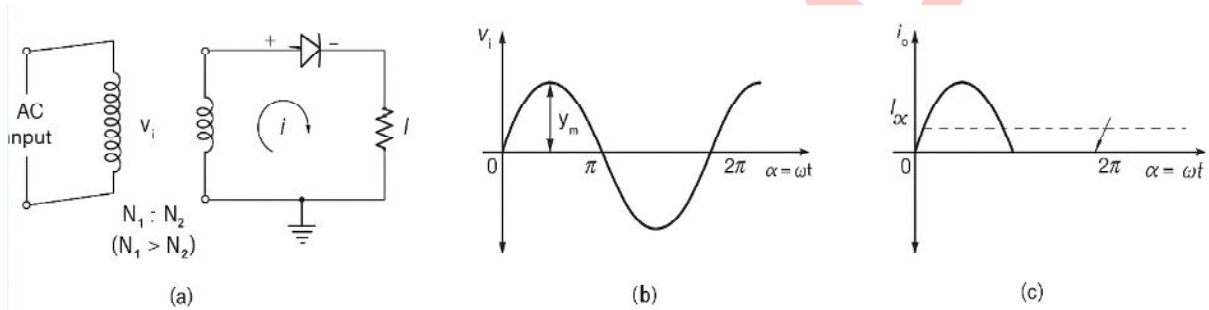
$$i = \begin{cases} I_m \sin \alpha & \text{where } 0 \leq \alpha \leq \pi \\ 0 & \text{where } \pi \leq \alpha \leq 2\pi \end{cases}$$

where,

$$\alpha = \omega t$$

and

$$I_m = \frac{V_m}{R_f + R_L}$$



DC Output Current

By definition, the dc value or the average value of a periodic function is given by the area of one cycle of the curve divided by the base. Expressed mathematically,

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i d\alpha$$

For the half-wave circuit under consideration

$$I_{DC} = \frac{1}{2\pi} \int_0^{\pi} I_m \sin \alpha d\alpha + \frac{2\pi}{\pi} \int_{\pi}^{2\pi} 0 d\alpha$$

$$\Rightarrow I_{DC} = \frac{I_m}{\pi}$$

RMS Output Current

By definition, the effective or rms value squared of a periodic function of time is given by the area of one cycle of the curve which represents the square of the function, divided by the base. Expressed mathematically,

$$I_{rms} = \sqrt{\left(\frac{1}{2\pi} \int_0^{2\pi} i^2 d\alpha \right)}$$

By use of equation, it follows that,

$$I_{rms} = \left(\frac{1}{2\pi} \int_0^{\pi} I_m^2 \sin^2 \alpha d\alpha \right)^{1/2}$$

$$\Rightarrow I_{\text{rms}} = \frac{I_m}{2}$$

RMS AC Output Current

The output of rectifier is combination of dc and ac components, so we can write

$$i = \text{DC current} + \text{AC current}$$

$$\Rightarrow i' = I_{\text{DC}} + i'$$

$$\Rightarrow i' = i - I_{\text{DC}} \\ = \text{AC output current}$$

Note that, $i_{\text{rms}} = \text{RMS value of total current (i)}$

$$i'_{\text{rms}} = \text{RMS value of AC current (i')}$$

$$\text{So, } i'_{\text{rms}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i'^2 d\alpha}$$

$$\Rightarrow I_{\text{rms}}'^2 = \frac{1}{2\pi} \int_0^{2\pi} (i - I_{\text{DC}})^2 d\alpha$$

$$\Rightarrow I_{\text{rms}}'^2 = \frac{1}{2\pi} \int_0^{2\pi} (i^2 - I_{\text{DC}}^2 - 2I_{\text{DC}} \cdot i) d\alpha \\ = \frac{1}{2\pi} \int_0^{2\pi} i^2 d\alpha + I_{\text{DC}}^2 \times \frac{1}{2\pi} \int_0^{2\pi} d\alpha - 2I_{\text{DC}} \times \frac{1}{2\pi} \int_0^{2\pi} i \cdot d\alpha$$

$$\Rightarrow I_{\text{rms}}'^2 = I_{\text{rms}}^2 + I_{\text{DC}}^2 - 2I_{\text{DC}}^2$$

$$\Rightarrow I_{\text{rms}}' = \sqrt{I_{\text{rms}}^2 - I_{\text{DC}}^2}$$

Note: An ac ammeter connected in series with the load shows I'_{rms} ; hence I'_{rms} is called reading of ac ammeter

Ripple Factor :

Although it is the purpose of a rectifier to convert alternating current into direct current, the simple circuit considered above neither achieve this nor, in fact, do any of the more complicated rectifier circuits have a truly constant output. What is accomplished is the conversion from an alternating current into a unidirectional current periodically fluctuating components still remaining in the output wave. It is for this reason that filters are frequently used in order to decrease these ac components. A measure of the fluctuating components is given by the ripple factor (r), which is defined as

$$r = \frac{\text{rms value of alternating components of wave}}{\text{average value of wave}}$$

This may be written as

$$r = \frac{I'_{\text{rms}}}{I_{\text{DC}}} = \frac{V'_{\text{rms}}}{V_{\text{DC}}}$$

$$\Rightarrow r = \frac{\sqrt{I_{\text{rms}}^2 - I_{\text{DC}}^2}}{I_{\text{DC}}}$$

$$\Rightarrow r = \sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{DC}}}\right)^2 - 1}$$

Equation gives the general expression to calculate ripple factor for any rectifier circuit.

For half-wave rectifier

$$r = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1}$$

$$\Rightarrow r = 2.21$$

Note:

- For half-wave rectifier rms ac component is 1.21 times the dc component or in other words we can say that ac component is stronger than dc component.
- Since ac component is unwanted so ripple factor should be smaller and ideally it should be equal to zero.

It is the average value of the product of the instantaneous voltage across secondary winding and instantaneous current through secondary winding.

Input Power (P_i):

It is the average value of the product of the instantaneous voltage across secondary winding and instantaneous current through secondary winding.

$$\begin{aligned} P_i &= \text{Average value of } (V_i \times i) \\ &= \frac{1}{2\pi} \int_0^{2\pi} V_i \times i d\alpha = \frac{1}{2\pi} \int_0^{2\pi} i(R_f + R_L) d\alpha \\ &= (R_f + R_L) \cdot \frac{1}{2\pi} \int_0^{2\pi} i^2 d\alpha \end{aligned}$$

$$\Rightarrow P_i = I_{rms}^2 (R_f + R_L)$$

Efficiency :

It is a measure of the ability of a rectifier to convert input AC power into dc power. Expressed mathematically

$$\begin{aligned} \eta &= \frac{\text{dc output power}}{\text{input power}} \\ \Rightarrow \% \eta &= \frac{P_{dc}}{P_i} \times 100\% = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_f + R_L)} \times 100\% \\ &= \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m^2}{4} (R_f + R_L)} \times 100\% = \frac{400}{\pi^2} \cdot \frac{R_L}{(R_f + R_L)} \% \\ \Rightarrow \% \eta &= 40.5\% \frac{R_L}{(R_f + R_L)} \end{aligned}$$

Remember: If a diode is ideal (i.e. $R_f = 0$) then half-wave rectifier can have maximum efficiency of 40.5%.



Q.41

Sol.

$$R_F = 20 \Omega, R_L = 1000 \Omega$$

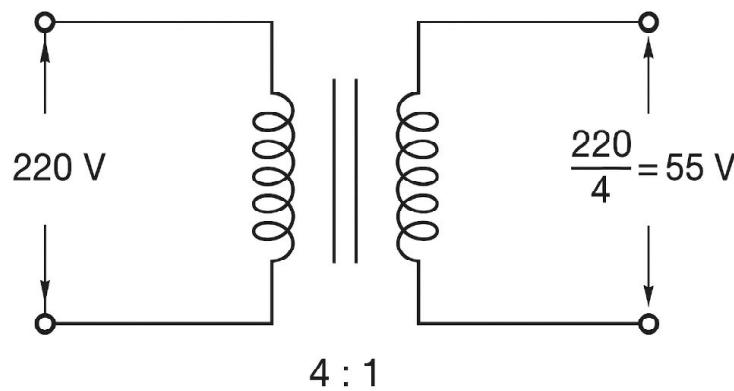
RMS voltage of secondary winding of transformer

$$V_{\text{rms}} = \frac{V_m}{\sqrt{2}} = 55$$

 $\Rightarrow$

$$V_m = 55\sqrt{2} = 77.78 \text{ V}$$

$$I_m = \frac{V_m}{R_F + R_L} = \frac{77.78}{20 + 1000} \\ = 0.076 \text{ A}$$



$$V_s = \frac{N_2}{N_1} \times V_p = \frac{1}{4} \times 220 \\ = 55 \text{ V} = \text{rms voltage}$$

(i)

$$\text{dc output current} = I_{\text{dc}} = \frac{I_m}{\pi} \\ = \frac{76}{\pi} = 24.2 \text{ mA}$$

$$V_{\text{dc}} = I_{\text{dc}} R_L$$

 $\Rightarrow$

$$V_{\text{dc}} = 24.2 \times 10^{-3} \times 1000 \\ = 24.2 \text{ V}$$

(ii) AC output current is I'_{rms}

$$I'_{\text{rms}} = r \times I_{\text{dc}}$$

 $\Rightarrow$

$$I'_{\text{rms}} = 1.21 \times 24.2 \\ = 29.28 \text{ mA}$$

AC output voltage is V'_{rms}

$$V'_{\text{rms}} = r \cdot V_{\text{dc}}$$



$$= 1.21 \times 24.2$$

$$= 29.28\text{V}$$

(iii) Since diode and R_L are in series, so dc diode current is same as dc output current

$$I_{\text{diode,dc}} = 24.2\text{mA}$$

$$V_{\text{diode,dc}} = -\frac{V_m}{\pi} = -\frac{77.78}{\pi} = -24.75\text{V}$$

(iv) $\text{PIV} = V_m = 77.78\text{V}$

(v) $\% \text{ Efficiency} = 40.5 \times \frac{R_L}{R_f + R_L}$

$$= 40.5 \times \frac{1000}{20 + 1000} = 39.7\%$$

$$\% \text{ Regulation} = \frac{R}{R_L} \times 100\%$$

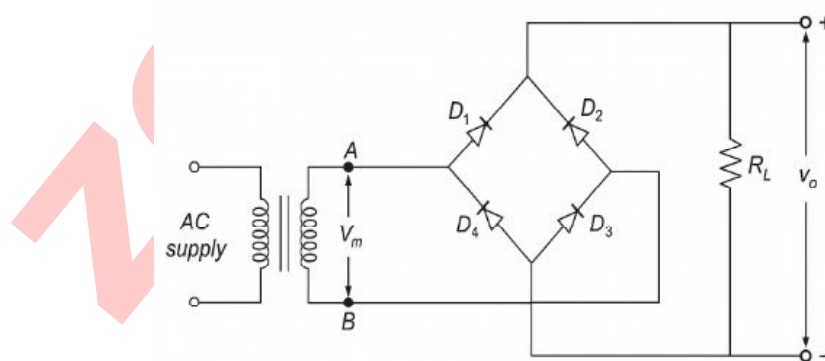
where, $R = R_{\text{sec}} + R_f = 0 + 20 = 20\ \Omega$

$$= \frac{20}{1000} \times 100\% = 2\%$$

Q.42

Sol. The fullwave rectifier circuit requires a center-tapped transformer where only one half of the total ac voltage of the transformer secondary winding is utilized to convert into dc output. We now consider a different configuration of fullwave rectifier circuit, called bridge rectifier, where entire AC voltage of the transformer secondary is used to convert into DC voltage.

Fig. shows a bridge rectifier circuit. There are four diodes D_1 , D_2 , D_3 and D_4 which form the four arms of the bridge. AC from transformer secondary is fed to two corners and the load resistance R_L is connected to other two corners.



During positive half-cycle of input point A is positive, diodes D_1 and D_3 are forward biased and diodes D_2 , D_4 are reverse biased then, the current flows through diode D_1 , the load R_L and through diode D_3 back to the negative polarity of the transformer secondary. During negative half cycle of input, point 'B' is more positive than point 'A', thus diodes D_2 , D_4 are forward biased and diode D_1 and D_3 are reverse biased, then the direction current flow will be through diode D_2 , load R_L and diode D_4 . In both cases the current flowing through resistor R_L is in same direction, thus it is unidirectional current and we obtain fullwave rectification.



Analysis

1. Instantaneous output current

$$i = \begin{cases} I_m \sin \alpha, & 0 < \alpha < \pi \\ -I_m \sin \alpha, & \pi < \alpha < 2\pi \end{cases}$$

where,

$$I_m = \frac{V_m}{2R_f + R_L}$$

2. DC Output Current

$$I_{DC} = \frac{2I_m}{\pi}$$

3. RMS Output Current

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

4. AC rms Output Current

$$I'_{rms} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

5. Ripple Factor

$$r = 0.483$$

6. Input Power (Pi)

$$P_i = I_{rms}^2 (2R_f + R_L)$$

7. Efficiency

$$\% \eta = 81 \times \frac{R_L}{2R_f + R_L} \%$$

8. DC Diode Voltage

Consider diode D_1 ,

V_{diode} = Instantaneous voltage across D_1

For $0 < \alpha < \pi$, diode D_1 is forward biased; so

$$V_{diode} = i.R_f \cong 0$$

For $\pi < \alpha < 2\pi$, diode D_1 is reverse biased, so it is open circuit and voltage across D_1 is

$$V_{diode} = V_i = V_m \sin \alpha$$

Thus,

$$V_{diode} = \begin{cases} 0, & 0 < \alpha < \pi \\ V_m \sin \alpha, & \pi < \alpha < 2\pi \end{cases}$$

Hence,

$$V_{diode, DC} = \text{Average value of } V_{diode}$$

$$= \frac{1}{2\pi} \int_0^{2\pi} V_{diode} d\alpha$$

$$V_{diode, DC} = -\frac{V_m}{\pi}$$

9. No Load DC Output Voltage

By applying KVL

$$V_{diode, DC} + V_{diode, DC} + V_{DCNL} = 0$$

$\therefore$

$$V_{diode, DC} = \frac{2V_m}{\pi}$$



10. Full Load DC Output Voltage

$$V_{DCNL} = \frac{2V_m}{\pi} = I_{DC}R$$

where,

$$R = R_{\text{secondary}} + 2R_f$$

Here dc voltage drop occurs across full secondary winding and across two diodes.

Also,

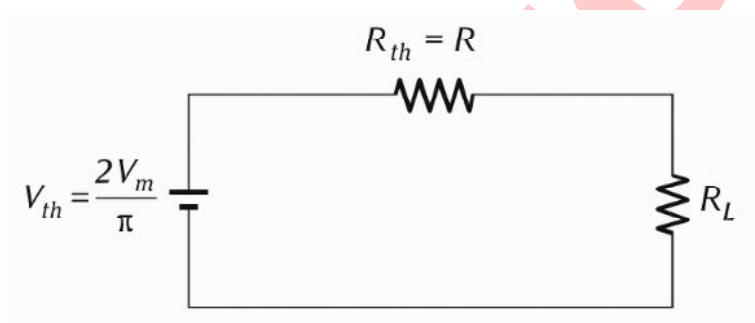
$$V_{DCFL} = I_{DC} \cdot R_L$$

11. Regulation

$$\% \text{ Regulation} = \frac{R}{R_L} \times 100\%$$

12. Thevenin's Equivalent Circuit

$$V_{OCFL} = \frac{2V_m}{\pi} - I_{DC}R$$



13. Peak inverse Voltage

$$PIV = |V_{\text{diode}}|_{\text{max}} \text{ in reverse bias condition}$$

$\Rightarrow$

$$PIV = |V_m \sin \alpha|_{\text{max}}$$

$\Rightarrow$

$$PIV = V_m$$

14. Transformer Utilization Factor

$$TUF = \frac{\text{DC output power}}{\text{AC rating of secondary winding}}$$

$$= \frac{I_{DC}^2 R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}} = \frac{8}{\pi^2} \cdot \frac{R_L}{(2R_f + R_L)}$$

$\Rightarrow$

$$TUF = 0.81\% \frac{R_L}{(2R_f + R_L)}$$

Note:

- For ideal diodes we get maximum $TUF = 0.81$.
- If transformers of identical ac rating are used in all three rectifiers then power will be maximum in bridge rectifier and minimum in other two.

15. Ripple Frequency

$$\text{Ripple frequency} = 2f_0$$



16. Angle of Conduction

If diodes are non-ideal overall conduction angle of bridge rectifier will be $(360^\circ - 4\theta)$ because each

diode conducts for $(180^\circ - 2\theta)$, where $\theta = \sin^{-1}\left(\frac{2V_\gamma}{V_m}\right)$.

17. Form Factor

$$F = \frac{I_{\text{rms}}}{I_{\text{DC}}} = 1.11$$

18. Peak Factor

$$\text{Peak factor} = \frac{I_M}{I_{\text{rms}}} = 1.41$$

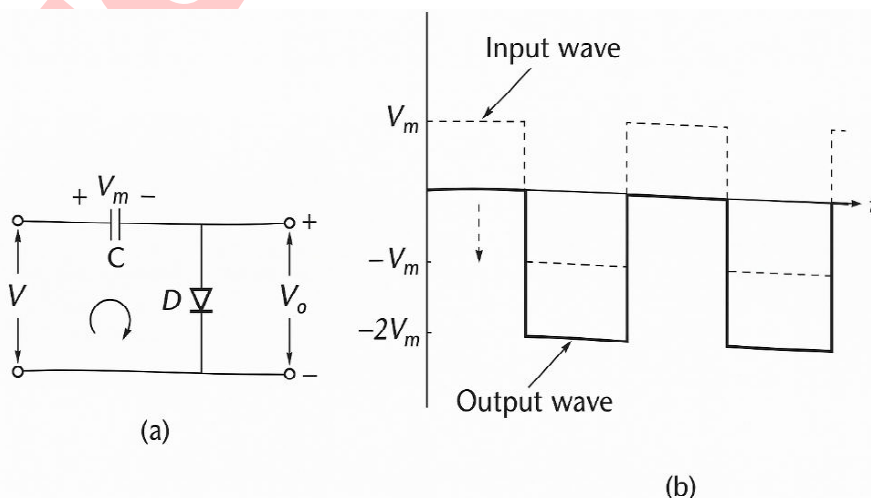
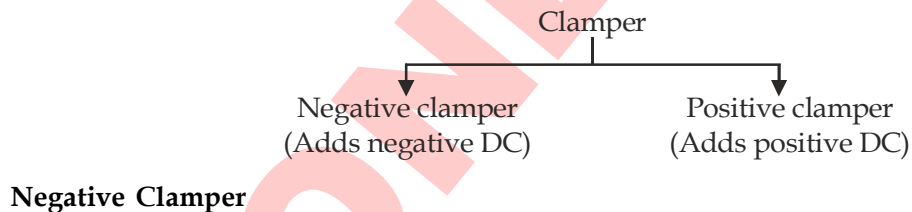
Advantages of Bridge Rectifier

- The current in both primary and secondary of transformer flows for entire cycle and hence for the given power output, power transformer of a small size and less cost may be used.
- A transformer without a center tap is used.
- Lower peak inverse voltage is required. The bridge circuit is thus suitable for high voltage applications. For example, if the peak output voltage is 50 V, the peak inverse voltage across each diode is also 50V. However, if a fullwave circuit were used, the peak inverse voltage would be 100 V.
- It provides greater TUF.

Q.43

Sol. Clamper :

A clamper is a network consisting of a diode, resistor, and capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal. A clamper is also used to reinsert or restore dc component into a waveform which has been lost after passing through a processing network such as an amplifier. Hence a clamper is also called dc inserter or dc restorer.



When input is positive, diode operates in forward bias and capacitor charges through diode. If diode is ideal it behaves as short circuit and therefore capacitor charges upto the peak input V_m .

When input becomes negative capacitor should discharge but discharge path is not available so capacitor voltage will continue to remain V_m . Therefore once capacitor is fully charged its voltage remains V_m , irrespective of the input being positive or negative.

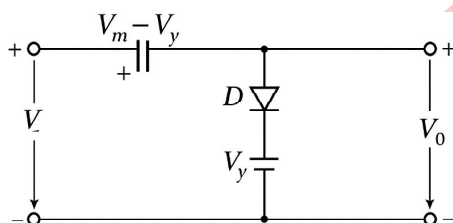
KVL:

$$-V_i + V_m + V_0 = 0$$

$$\Rightarrow V_0 = V_i - V_m$$

$$\Rightarrow V_0 = V_i + (-V_m)$$

Hence circuit adds dc voltage of $-V_m$. So output will be a square waveform for given input whose value varies from 0 to $-2V_m$. Positive peak of output waveform touches 0 volt level or positive peak gets clamped to 0 volt. Since a negative clamper is clamping positive peak to 0 volt so it is also called positive peak clamper.



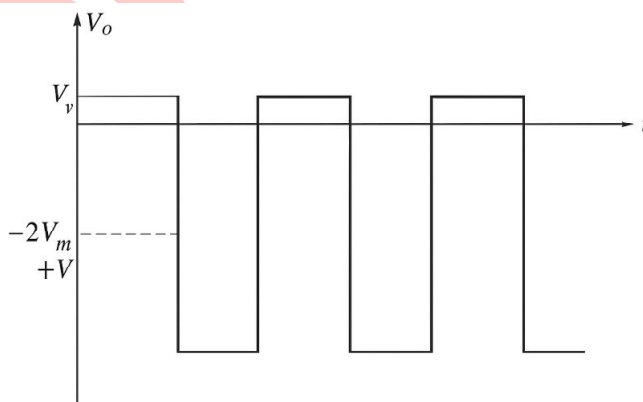
- If diode has cut-in voltage V_γ then it should be replaced with series connection of ideal diode and battery V_γ

When input is positive capacitor charges through diode upto a maximum voltage of $V_m - V_\gamma$

$$\therefore V_0 = V_i - (V_m - V_\gamma)$$

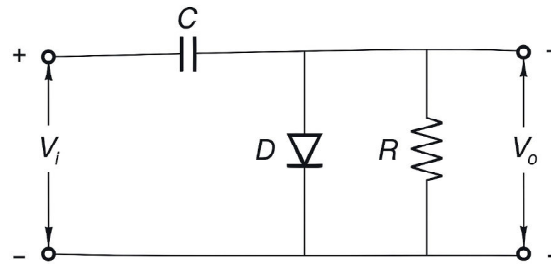
$$\Rightarrow V_0 = V_i + (-V_m + V_\gamma)$$

Hence circuit adds dc voltage equal to $-(V_m - V_\gamma)$.



Hence when diode is non-ideal negative clamper will clamp positive peak to V_γ

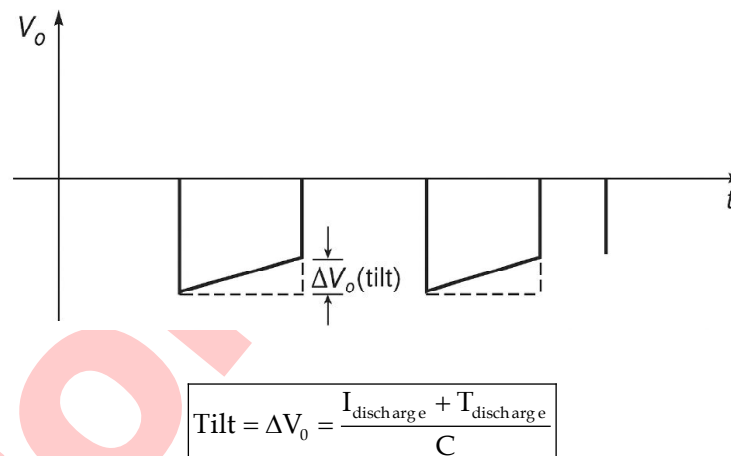
Drawbacks of Ideal Clamper



- As capacitor does not have discharge path so its voltage can not decrease even when the peak ac input is reduced which makes this clamping operation imperfect.
- To overcome the above drawback a sufficiently large resistance should be connected in shunt with the diode such a circuit is called practical clamper.
- When peak input is reduced capacitor slowly discharges through resistance R and after a finite time interval its voltage becomes equal to new peak value.
- R should be large enough so that capacitor does not have undesired discharging when peak input is stable.

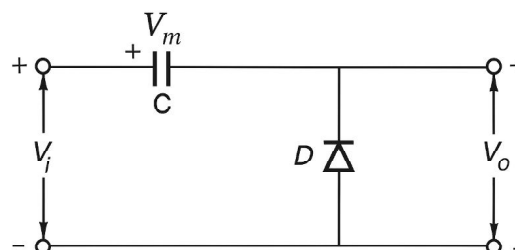
Drawback of Practical Clamper

During negative cycle diode will be in off condition then capacitor slowly discharges through resistance R as a result capacitor voltage decreases and tilt appear in output waveform.



Where discharging current is approximated as

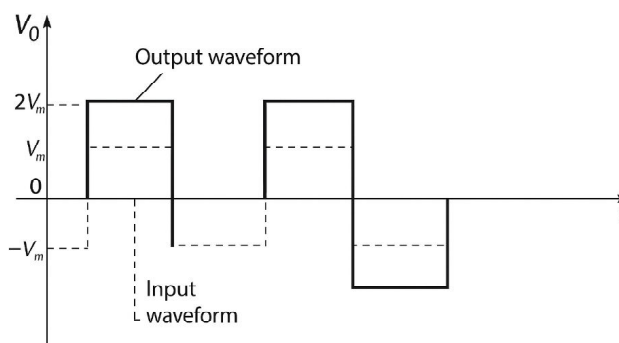
$$I_{\text{discharge}} = \frac{2V_m}{R}$$

Positive Clamper:

- When input is negative diode gets forward biased and capacitor charges through diode upto peak input V_m .
- When input becomes positive capacitor will not be able to discharge as discharge path is not present; therefore voltage across the capacitor remains V_m irrespective of input being $+V_m$ or $-V_m$.

KVL:

$$V_0 = V_1 + V_m$$

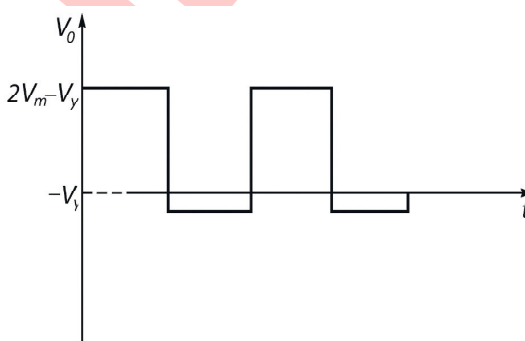


- Negative peak of output gets clamped to 0 volt therefore positive clamper is also called negative peak clamper.
- If diode has cut-in voltage V_γ then capacitor charges to a voltage $(V_m - V_\gamma)$.

Applying KVL again

$$V_0 = V_i + (V_m - V_\gamma)$$

Hence added dc voltage is $(V_m - V_\gamma)$.



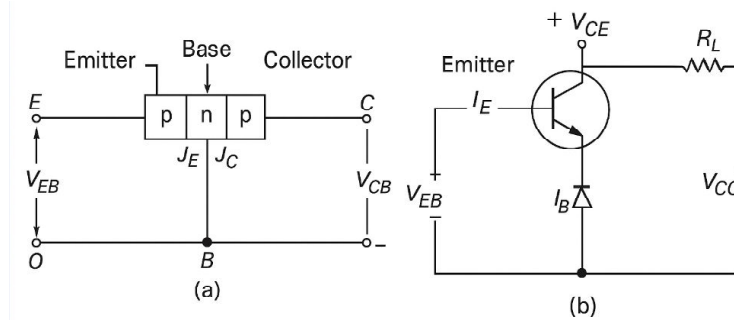
Here negative peak gets clamped to $-V_\gamma$.

Q.44

Sol. The Common Base Configuration

In Fig. a p-n-p transistor is shown in a grounded-base configuration. This circuit is also referred to as a Common Base (CB) configuration, since the base is common to the input and output circuits. For a p-n-p transistor the largest current components are due to holes. Since holes flow from emitter to collector and down towards ground out of the base terminal, then referring to the polarity conventions of Fig. We have seen that I_E is positive, I_C is negative and I_B is negative for a forward-biased emitter junction, V_{EB} is positive and for a reverse-biased collector junction, V_{CB} is negative. For an n-p-n transistor all current and voltage polarities are negative of those for a p-n-p transistor.





We may completely describe the transistor of Fig. by the following two relations, which give the input voltage V_{EB} and output current I_C in terms of the output voltage V_{CB} and input current I_E :

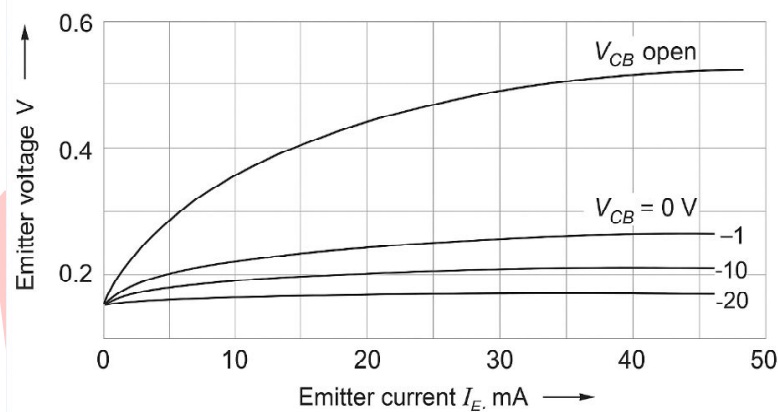
$$V_{EB} = \phi_1(V_{CB}, I_E)$$

$$I_C = \phi_2(V_{CB}, I_E)$$

(This equation is read, " I_C is some function of ϕ_2 of V_{CB} and I_E ").

Input Characteristics

- A qualitative understanding of form of input and output characteristics is not difficult if we consider the fact that the transistors consists of two diodes placed in series "back to back" (with two cathodes connected together).
- In the active region the input diode (emitter to base) is biased in forward direction. The input characteristics of Fig. represent simply the forward characteristics of emitter to base diode for various collector voltages.
- From input characteristics of Fig. we conclude that there exists a cut-in, offset, or threshold voltage V_γ , below which the emitter current is very small. In general, V_γ is approximately 0.1 V for germanium and 0.6 V for Si transistors.

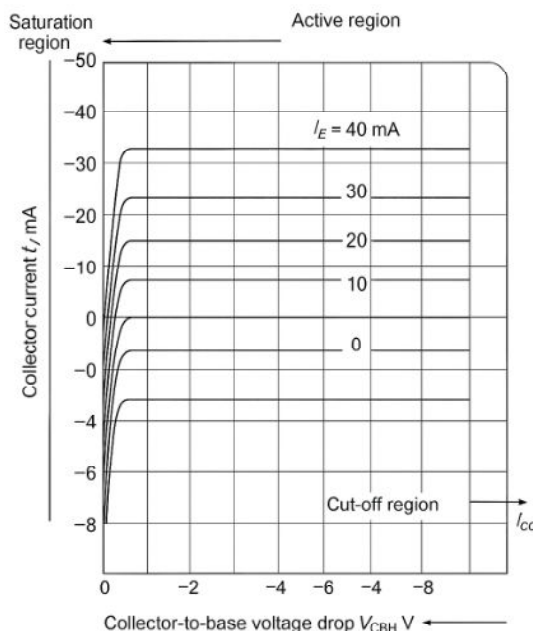


- If we increase the magnitude of collector voltage, by Early effect, it causes increase in collector current when V_{EB} is kept constant. Thus curve shifts downward as $|V_{CB}|$ increases.
- The curve with collector open represents the characteristics of forward-biased emitter diode. When the collector is shorted to base, the emitter current increases for a given V_{EB} since the collector removes minority carriers from the base, and hence base can attract more holes from emitter. This means that the curve with $V_{CB} = 0$ is shifted downwards from the collector characteristics marked " V_{CB} open".



Output Characteristics

- The relation of Equation is given in Fig. for a typical p-n-p germanium transistor and a plot of collector current I_C versus collector to base voltage drop V_{CB} with emitter current I_E as a parameter. The curves of Fig. are known as output, or collector, static characteristics.



- The collector-to-base diode is normally biased in reverse direction. If $I_E = 0$, the collector current is $I_C = I_{CO}$. For other values of I_E , the output diode reverse current is augmented by a fraction of input diode forward current which reaches the collector. Note that I_{CO} is negative for p-n-p transistor and positive for npn transistor.

Active Region

- In this region the collector junction is biased in reverse direction and the emitter junction in forward direction.
- If emitter current is zero then collector current is small and equals the reverse saturation current I_{CO} of collector junction considered as a diode.
- Now if forward emitter current I_E is caused to flow in emitter circuit then a fraction $-\alpha I_E$ of this current will reach the collector and I_E will be given by following equation:

$$I_C = \alpha I_E + I_{CO}$$

- In the active region, the collector current is essentially independent of collector voltage and depends only upon emitter current. However, due to Early effect there is small (perhaps 0.5 percent) increase in $|I_C|$ with $|V_{CB}|$.
- Because α is less than, but almost equal to unity, the magnitude of the collector current is (slightly) less than that of emitter current.

Saturation Region

The region to the left of the ordinate, $V_{CB} = 0$, and above the $I_E = 0$ characteristics in which both emitter and collector junctions are forward-biased, is called the saturation region. We say that "bottoming" has taken place because the voltage has fallen near bottom of the characteristics where $V_{CB} \approx 0$. Actually, V_{CB} is slightly positive (for p-n-p transistor) in this region, and this forward biasing of the collector accounts for large change in collector current with small changes in collector voltage.

Cut-off Region

The characteristic for $I_E = 0$ passes through the origin, but is otherwise similar to other characteristics. This characteristic is not coincident with voltage axis, though the separation is difficult to show because I_{CO} is only a few nanoamperes or microamperes. The region below and to the right of the $I_E = 0$ characteristics, for which the emitter and collector junctions are both reverse-biased, is referred to as cut-off region.

Q.45

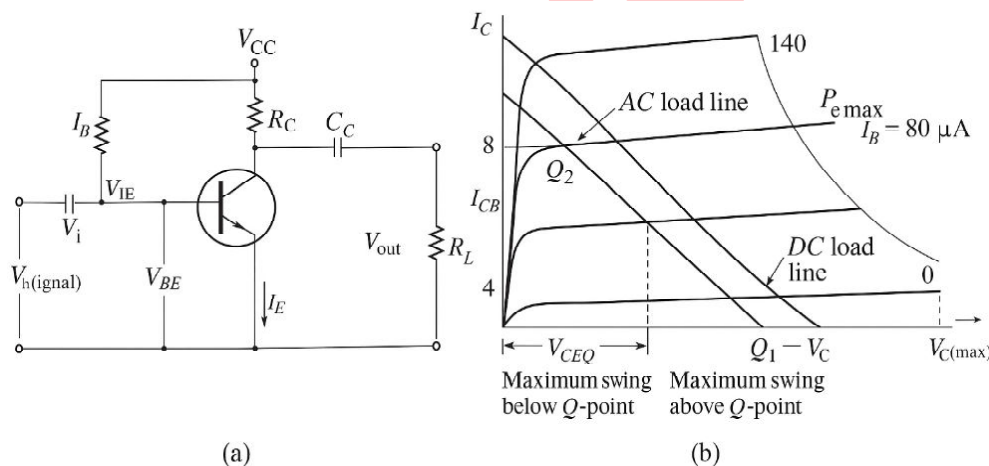
Sol. Biasing refers to providing appropriate DC voltages and DC currents to an electronic device to operate it in a desired way. Biasing of BJT is done for following purposes:

- (i) To operate the BJT in active region so that it can be used as an amplifier.
 - (ii) To maintain I_C stable so that operating point does not drift and thermal runaway cannot take place.
- Commonly used biasing circuits are:

- (i) Fixed bias circuit.
- (ii) Collector to base bias circuit.
- (iii) Self bias circuit.

Fixed Bias Circuit

In Fig., the base current is derived from supply voltage V_{CC} by resistor R_B . This type of biasing is called fixed bias as V_{CC} and R_B are fixed quantities.



The operating point Q_1 is chosen on load line for a particular base current I_B as shown in Fig. By applying KVL in input loop, we have

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \dots(3.8)$$

Similarly by applying KVL in output loop, we have

$$V_{CE} = V_{CC} - I_C R_C \quad \dots(3.9)$$

where,

$$I_C = \beta I_B + (1 + \beta) I_{CO} \approx \beta I_B$$

Hence from equations (3.8) and (3.9) we can calculate Q-point (V_{CEQ} , I_{CQ}) for a fixed I_B .

Stability Factor

From equation (3.8), we have

$$\frac{\partial I_B}{\partial I_C} = 0$$

So, stability factor, from equation (3.7), is

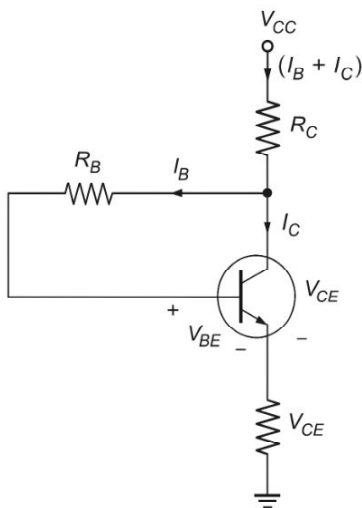
If $\beta = 50$, the stability factor is 51 and the collector current is 51 times that of I_{CO} , reverse saturation current. Hence we see that the stability factor for a fixed bias circuit is very high, so it will be the least stable biasing arrangement,

Q.46

Sol. Collector to Base Bias Circuit

An improvement in bias stability is obtained if tapping for bias is taken from the collector terminal instead of from the collector supply point as shown in Fig.

Applying KVL in input loop, we have



$$-V_{CC} + (I_B + I_C)R_C + I_B R_B + V_{BE} = 0 \quad \dots(3.11)$$

Using $I_C \approx \beta I_B$, we have

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{\left(1 + \frac{1}{\beta}\right)R_C + R_B} \quad \dots(3.12)$$

Now applying KVL in the output loop, we have

$$-V_{CC} + R_C(I_B + I_C) + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - R_C(I_B + I_C) \quad \dots(3.13)$$

With the help of equations (3.12) and (3.13) we can calculate operating point for given biasing circuit.

Stability Factor

To calculate stability factor, differentiating equation (3.11) with respect to I_C ; we have

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_B + R_C}$$

Putting above value in equation (3.7), we have

$$S = \frac{\beta + 1}{1 + \beta \frac{R_C}{R_B + R_C}}$$

Advantage

Here stability factor is smaller than $(\beta + 1)$, hence an improvement in stability is obtained over fixed bias circuit.

Disadvantage

- Stability factor depends upon R_C . If R_C becomes smaller or zero then stability factor becomes very large and I does not remain stable.

Resistance R_b connected from collector to base causes negative feedback due which voltage gain of the amplifier circuit decreases.

Q.47

Sol. Self-Bias, Emitter Bias, or Voltage-Divider Bias

If the collector resistance R_C is very small, for example, in a transformer-coupled circuit, then from equation (3.14) we see that there is no improvement in stabilization in collector-to-base bias circuit over the fixed-bias circuit. A circuit which can be used even if there is zero DC resistance in series with the collector terminal is self-biasing configuration of Fig. 3.6 (a). The current in resistance R_e in emitter lead causes a voltage drop which is in direction of reverse-biasing the emitter junction. Since this junction must be forward-biased, the base voltage is obtained from supply through R_1, R_2 network. Note that if $R_b = R_1 \parallel R_2 \rightarrow 0$, then base to ground voltage V_{BN} is independent of I_{CO} . Under these

circumstances we may verify that $S = \frac{\partial I_C}{\partial I_{CO}} \rightarrow 1$. For best stability R_1 and R_2 must be kept as small as possible.

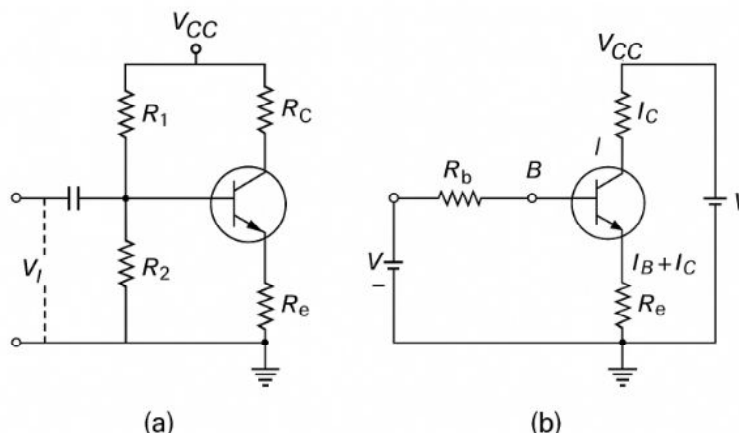


Figure- (a) A self-bias circuit (b) Simplification of the base circuit in Fig. (a) by use of Thevenin's theorem

The given self-bias circuit can be simplified by using Thevenin's theorem. Thevenin's equivalent can be found between base and ground as shown in Fig. 3.6 (b).

Here,
$$V = \frac{R_2}{R_1 + R_2} V_{CC} \quad \dots(3.15)$$

and
$$R_b = \frac{R_1 R_2}{R_1 + R_2} \quad \dots(3.16)$$

Now applying KVL in input loop,

$$-V + I_B R_b + V_{BE} + (I_B + I_C) R_e = 0 \quad \dots(3.17)$$

By using $I_C \approx \beta I_B$, we have

$$I_B = \frac{V - V_{BE}}{R_b + \left(1 + \frac{1}{\beta}\right) R_e} \quad \dots(3.18)$$

Again applying KVL in output loop, we have

$$\begin{aligned} -V_{CC} + I_C R_C + (I_B + I_C) R_e + V_{CE} &= 0 \\ \Rightarrow V_{CE} &= V_{CC} - I_C (R_C + R_e) - I_B R_e \end{aligned} \quad \dots(3.19)$$

By using equations (3.18) and (3.19) we can easily calculate operating point for self-bias circuit.

Stability Factor

To calculate stability factor, differentiate equation (3.17) with respect to I_C

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_e}{R_b + R_e}$$

Putting above value in equation (3.7), we have

$$S = \frac{1 + \beta}{1 + \frac{\beta R_e}{R_b + R_e}} \quad \dots(3.20)$$

- Note that S varies between 1 for small R_b/R_e and $1 + \beta$ for $R_b/R_e \rightarrow \infty$.
- Smaller the value of R_b , better is stabilization. Note that even if R_b approaches zero, the value of S can not be reduced below unity. Hence I_C always increases more than I_{CO} .
- As R_b is reduced while Q-point is held fixed, the current drawn in R_1, R_2 network from supply V_{CC} increases.
- Also, if R_e increased while R_b is held constant, then to operate at the same quiescent current, the magnitude of V_{CC} must be increased.
- In either case a loss of power (decreased efficiency) is disadvantage which accompanies the improvement in stability.
- In order to avoid the losses of AC (signal) gain because of feedback caused by R_e , this resistance is often bypassed by a large capacitance ($> 10 \mu F$), so that its reactance at frequencies under consideration is very small.

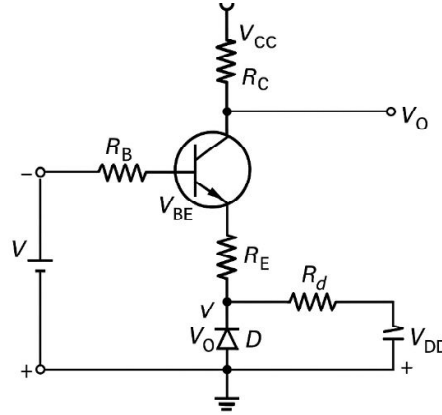
Q.48

Sol. Bias Compensation

The collector-to-base circuit and the self-bias circuit are used to limit the variations in operating collector current I_C caused by variations in I_{CO} , V_{BE} and β . These circuits are examples of feedback amplifiers, where it is found that as a consequence of feedback there is reduction in amplification of signal. If this loss in signal gain is intolerable in any particular application, then it is often possible to use compensating techniques to reduce the drift in operating point. Very often both stabilization and compensation techniques are used to provide maximum bias and thermal stabilization.

Diode Compensation for V_{BE}

A circuit utilizing self-bias stabilization technique and diode compensation is shown in Fig. The diode is kept biased in forward direction by source V_{DD} and resistance R_d . If diode is of same material and type as the transistor is, then voltage V_0 across diode will have same temperature coefficient ($-2.5 \text{ mV}/^\circ\text{C}$) as the base to emitter voltage V_{BE} have.



If we write KVL around the base circuit of Fig., then

$$I_C = \frac{\beta [V - (V_{BE} - V_0) + (R_b + R_C)(\beta + 1)I_{CO}]}{R_b + R_C(1 + \beta)} \quad \dots(3.21)$$

Since V_{BE} tracks V_0 with respect to temperature, it is clear from Equation (3.21) that I_C will be insensitive to variations in V_{BE} .

Diode Compensation for I_{CO}

The diode compensation circuit shown in Fig. (3.8) offers stabilization. against variations in I_{CO}

If the diode and transistor are of same type material, then the reverse saturation current I_O of diode will increase with temperature at the same rate as the transistor collector saturation current I_{CO} . From Fig. (3.8) we have,

$$I = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} = \text{constant} \quad \dots(3.22)$$

Since the diode is reverse biased, it follows that the current through diode is I_O . The base current is $I_b = I - I_O$; so we have

$$I_C = \beta I - \beta I_O + (1 + \beta) I_{CO} \quad \dots(3.23)$$

We see from Equation (3.23) that if $\beta \gg 1$ and if I_O of diode and I_{CO} of transistor track each other over the desired temperature range, then I_C remains essentially constant.

Thermistor and Sensistor Compensation

There is a method of transistor compensation which involves the use of temperature-sensitive resistive elements rather than diodes or transistors. The thermistor has negative temperature coefficient, its resistance decreases exponentially with increase in temperature. The circuit of Fig. uses a thermistor R_T to minimize the increase in collector current due to changes in I_{CO} , V_{BE} or β with temperature. As temperature rises, R_T decreases and the current fed through R_T into R_E increases. Since the voltage drop across R_E is in direction to reverse-bias the transistor, the temperature sensitivity of R_T acts so as to tend to compensate the increase in I_C due to temperature.



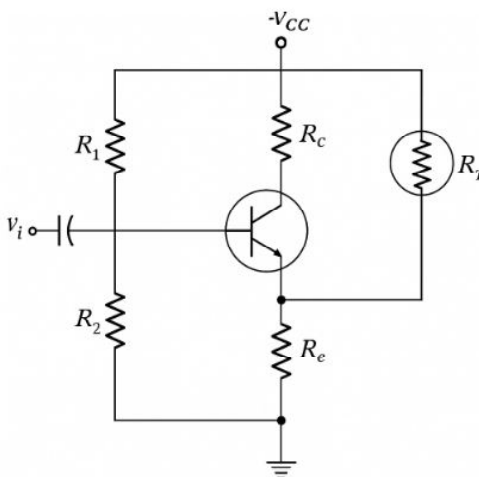


Figure: Thermistor compensation of the increase in I_C with temperature

An alternate configuration using thermistor compensation is to move R_T from its position in Fig. and place it across R_2 . As temperature increases, the drop across R_T decreases, and hence the forward-biasing base voltage is reduced. This behaviour will tend to offset the increase in collector current with temperature.

Instead of thermistor, it is possible to use a temperature-sensitive resistor with positive temperature coefficient such as a metal, or the sensistor. In circuit of Fig. (with R_T removed), temperature compensation may be obtained by placing a sensistor either in parallel with R_1 or in parallel with (or in place of) R_e .

Q.49

Ans. **Series-Shunt Configuration**

The configuration of an ideal series-shunt feedback amplifier is shown in figure. The feedback circuit samples the output voltage and produces a feedback voltage V_{fb} which is in series with the input signal voltage V_i . We can recognize the series connection on input and shunt connection on output for this configuration.

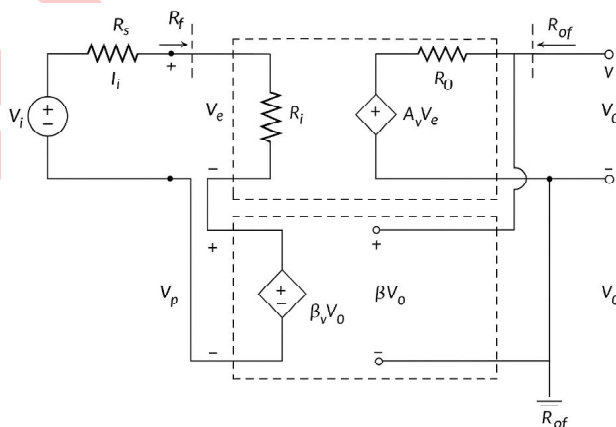


Figure: Ideal series-shunt feedback topology

If the output of the feedback network is an open circuit, then the output voltage is

$$V_o = A_v V_e \quad \dots(8.16)$$



and the feedback voltage is

$$V_{fb} = \beta V_0 = \beta_v V_0 \quad \dots(8.17)$$

The error voltage, assuming the source resistance R_s is negligible, is

$$V_e = V_i - V_{fb} \quad \dots(8.18)$$

Combining equations (8.16), (8.17) and (8.18) we find the closed-loop voltage transfer function as

$$A_{vf} = \frac{V_0}{V_i} = \frac{A_v}{(1 + \beta_v A_v)} \quad \dots(8.19)$$

Equation (8.19) is the closed-loop voltage gain of feedback amplifier.

The input resistance including feedback is denoted by R_{if} . Starting with equation (8.18), using equation (8.16) and (8.17), we find that

$$\begin{aligned} V_i &= V_e + V_{fb} = V_e + \beta_v V_0 \\ &= V_e + \beta_v (A_v V_e) \end{aligned}$$

or

$$V_e = \frac{V_i}{(1 + \beta_v A_v)} \quad \dots(8.20)$$

The input current is

$$I_i = \frac{V_e}{R_i} = \frac{V_i}{R_i (1 + \beta_v A_v)} \quad \dots(8.21)$$

and the input resistance with feedback is then

$$R_{if} = \frac{V_i}{I_i} = R_i (1 + \beta_v A_v)$$

Equation (8.22) shows that a series input connection results in an increased input resistance compared to that of the basic voltage amplifier. A large input resistance is a desirable property of a voltage amplifier.

The output resistance of the feedback circuit can be determined from the equivalent circuit in figure (8.11). The input signal voltage source is set equal to zero (a short-circuit), and a test voltage is applied to the output terminals.

From the circuit, we see that,

$$V_e + V_{fb} = V_e + \beta_v V_x = 0$$

or

$$V_e = -\beta_v V_x \quad \dots(8.23)$$

The output current is

$$I_x = \frac{V_x - A_v V_e}{R_0} = \frac{V_x - A_v (-\beta_v V_x)}{R_0}$$

$\Rightarrow$

$$I_x = \frac{V_x + A_v \beta_v V_x}{R_0}$$

and the output resistance, including feedback resistance is

$$R_{of} = \frac{V_x}{I_x} = \frac{R_0}{(1 + \beta_v A_v)} \quad \dots(8.25)$$

Equation (8.25) shows that a shunt output connection results in a decreased output resistance compared to that of the basic voltage amplifier. A small output resistance is a desirable property of a voltage amplifier.



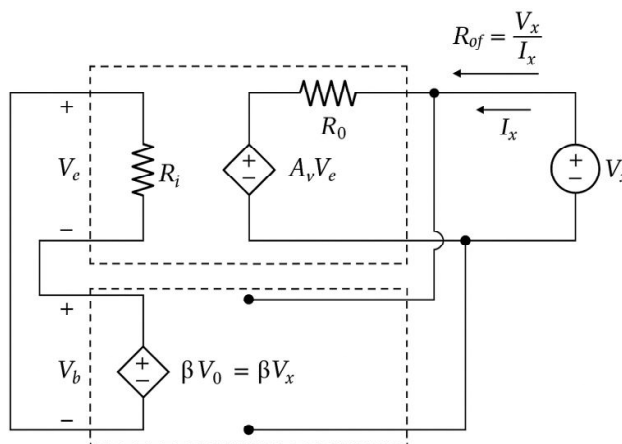
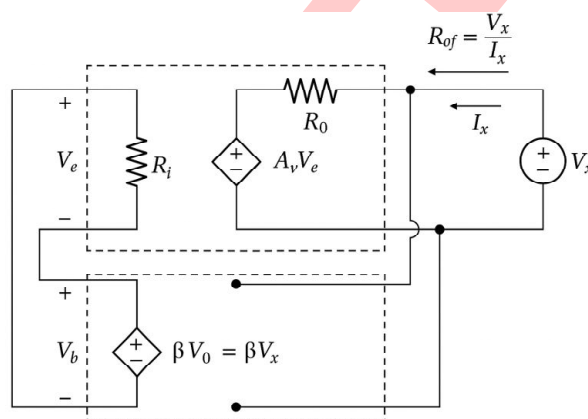


Figure: (Ideal series-shunt feedback configuration for determining output resistance)

Q.50

Sol. **Series-Series Configuration:**

The configuration of an ideal series-series feedback amplifier in figure. The feedback circuit samples a portion of the output current and converts it to a voltage.



Assuming the output is essentially a short-circuit, the output current is

$$I_0 = A_g V_e \quad \dots(8.36)$$

and the feedback voltage is

$$V_{fb} = \beta_z I_0 \quad \dots(8.37)$$

The input signal voltage, neglecting the effect of R_{S_i} is

$$V_1 = V_2 + V_{fb} \quad \dots(8.38)$$

Combining these equations, as we have in previous analysis, yields the closed-loop current-to-voltage transfer function

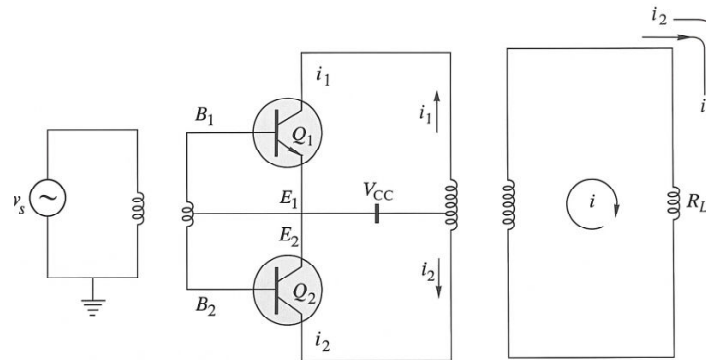
$$A_{gf} = \frac{I_0}{V_i} = \frac{A_g}{(1 + \beta_z A_g)} \quad \dots(8.39)$$

The units of the transfer function given by equation (8.39) are amperes/volt, or conductance. We may note that the term $\beta_z A_g$ is dimensionless. This particular feedback circuit is therefore called a transconductance amplifier.

The input resistance is given by equation (8.22) and the output resistance is given by equation (8.35).

Q.51

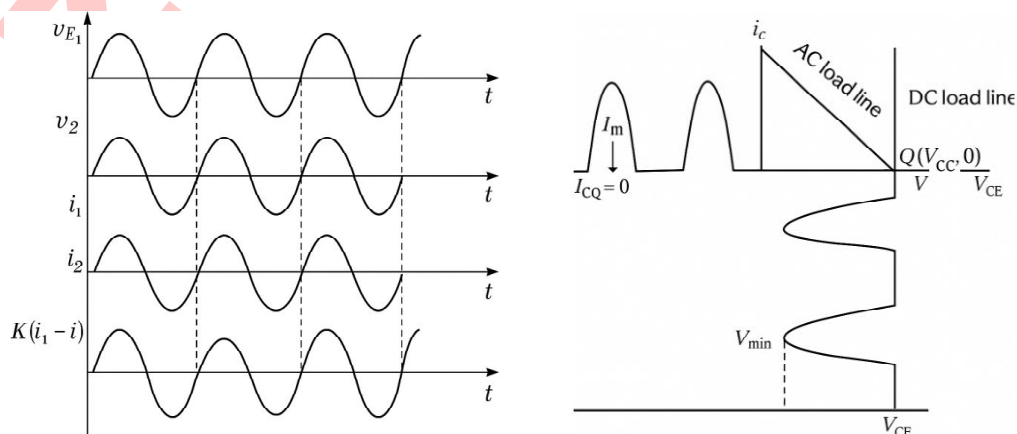
Sol. • Fig. shows the transformer coupled class-B push-pull amplifier.



- To obtain sinusoidal output we need two transistors in class-B amplifier.
- As winding of the transformer is short circuited for DC so base of transistor Q_1 gets short circuited to emitter of transistor Q_1 and similarly base and emitter of Q_2 are also short-circuited with respect to DC, therefore,

$$V_{BE_1} = V_{BE_2} = 0 \quad \dots(9.16)$$

- Hence if AC input is not applied then both transistors remain off, so power dissipation in Q_1 and Q_2 will be zero.
- When AC input (v_s) is applied, an AC voltage appears at B_1 (base of Q_1) and B_2 (base of Q_2) which is equal in magnitude but opposite in sign.
- During one half-cycle of v_s , AC voltage at B_1 is positive and at B_2 is negative. So in this case Q_1 begins conduction whereas Q_2 remains off. As a result current i_1 flows upward in primary winding of output transformer.
- During second half-cycle of v_s voltage at B_1 becomes negative and voltage at B_2 becomes positive; so Q_2 starts conduction and Q_1 remains turned off. As a result current i_2 flows downward in the primary of output transformer.
- As i_1 and i_2 flows in opposite directions, the resulting current in secondary winding of output transformer will be bi-directional and sinusoidal as shown in Fig.



Conversion Efficiency

From Fig.,

$$V_m = V_{CC} - V_{min}$$

and

$$I_{CQ} = I_m$$

So, AC output power

$$P_{AC} = \frac{1}{2}(V_{CC} - V_{min})I_m \quad \dots(9.17)$$

Under the effect of input, each transistor has half-sinusoidal collector current therefore the average or DC collector current of each transistor will be I_m / π . So DC power drawn by each transistor will

be equal to $\frac{V_{CC} \cdot I_m}{\pi}$. Hence total DC power obtained from biasing supply is given as

$$P_{DC} = \frac{2 \cdot V_{CC} I_m}{\pi} \quad \dots(9.18)$$

Using equations (9.17) and (9.18), we have efficiency of class-B transformer coupled amplifier as

$$\% \eta = \frac{P_{DC}}{P_{DC}} \times 100\% = \frac{\frac{1}{2}(V_{CC} - V_{min})I_m}{\frac{2V_{CC}I_m}{\pi}} \times 100\%$$

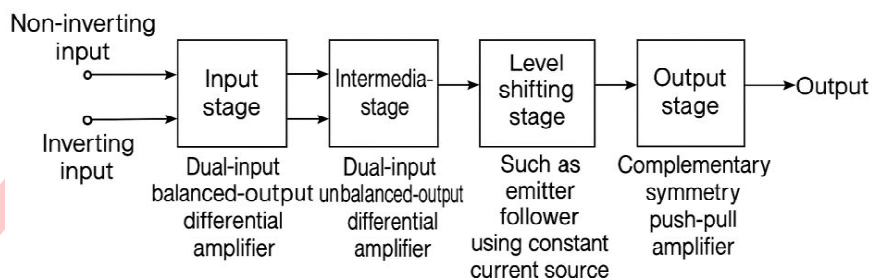
$$\% \eta = \left(1 - \frac{V_{min}}{V_{CC}}\right) \times 78.5\% \quad \dots(9.19)$$

Remember: If $V_{min} = 0$ or signal variation is maximum then class-B push pull amplifier has maximum efficiency and that is equal to 78.5%.

However, the electronics of op-amp is described where various stages of op-amp are discussed.

Q.52

Sol. Block Diagram Representation of A Typical Op-Amp



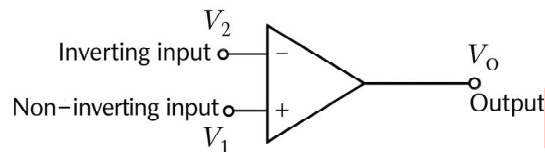
- An operational-amplifier is a direct-coupled high gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output.
- The input stage is the dual-input, balanced-output differential amplifier. This stage generally provides most of the voltage gain and also establishes the input resistance of the op-amp.
- The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. In most amplifiers the intermediate stage is dual input, unbalanced (single-ended) output.
- As direct coupling is used, so the DC voltage at the output of the intermediate stage is well above ground potential. Therefore, generally, the level translator (shifting) circuit is used after intermediate stage to shift the DC level at the output of intermediate stage downward to zero volts with respect to ground.



- The final stage is usually a push-pull complementary amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capability of the op-amp. A well-designed output stage also provides low output resistance.

Note: The operational amplifier is a versatile device that can be used to amplify DC as well as AC input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication, and integration. Thus the name operational amplifier stems from its original use for these mathematical operations.

Schematic Symbol



Given an op-amp schematic diagram, we can save time by using a schematic symbol for the entire op-amp circuit. Fig. shows the most widely used symbol for a circuit with two inputs and one output. For simplicity, power supply and other pin connections are omitted. Since the input differential stage of the op-amp is designed to be operated in the differential mode, the differential inputs are designated by the (+) and (-) notations. The (+) input is non-inverting input. An AC signal or DC voltage applied to this input produces an inphase (or same polarity) signal at the output. On the otherhand, the (-) input is inverting input because an AC signal or DC voltage applied to this input produces an 180° out- of-phase (or opposite polarity) signal at the output.

In figure

V_1 = Voltage at the non-inverting input (volts)

V_2 = Voltage at the inverting input (volts)

V_0 = V Output voltage (volts)

Here, $V_0 = A(V_1 - V_2)$... (10.1)

All these voltages are measured with respect to ground.

where, A = Large-signal voltage gain, which is specified on the data sheet for an op-amp.

Q.53

Sol. Inverting Amplifier :

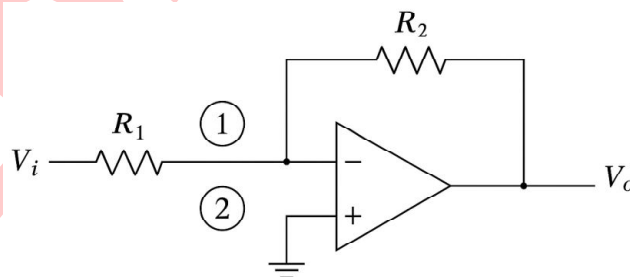


Fig. shows an inverting configuration. We speak of R_2 for applying negative feedback, if R_2 were connected between terminals 3 and 2; we would have called this positive feedback. Vo Note also that R_2 closes the loop around the op-amp.

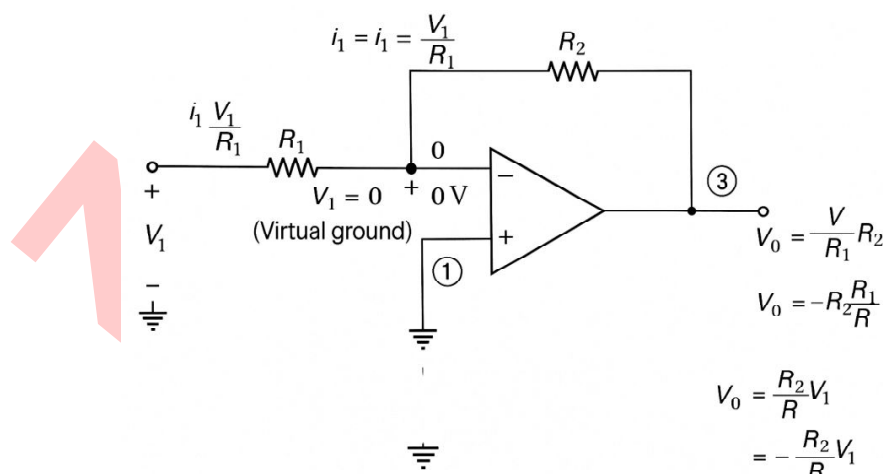
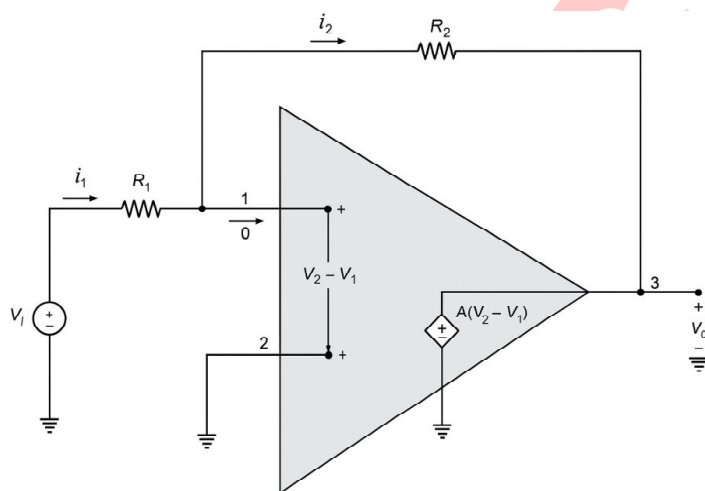
We analyze the circuit in Fig. by considering an ideal equivalent circuit shown in Fig. 10.11 (a). The closed-loop voltage gain, or simply the voltage gain is defined as

$$A_v = \frac{V_0}{V_i}$$

The open loop gain A is very large (ideally infinite). If we assume that the circuit is "working" and producing a finite output voltage at terminal 3, then the voltage between the op-amp input terminals should be negligibly small and ideally zero. Specifically, if we call the output voltage as V_0 then

$$V_2 - V_1 = \frac{V_0}{A} = 0 \quad \dots(10.17)$$

It follows that the voltage at inverting input terminal (V_1) is given by $V_1 = V_2$. This is because gain A approaches infinity, the voltage V , approaches and ideally equals to V_2 . We speak of this as the two input terminals "tracking each other in potential". We also speak of "virtual short circuit" that exists between two input terminals. Here the word virtual should be emphasized, and one should not make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A virtual short-circuit means that whatever voltage is at 2 will automatically appear at 1 due to infinite gain A . But terminal 2 happens to be connected to ground; thus $V_2 = 0$ and $V_1 = 0$. We speak of terminal 1 as being virtual ground that is, having zero voltage but not physically connected to ground.



Current i_1 through R_1 can be given as

$$i_1 = \frac{V_i - V_1}{R_1} = \frac{V_i - 0}{R_1} = \frac{V_i}{R_1}$$



Where will this current go? It cannot go into op-amp, since an ideal op-amp has infinite input impedance and hence draws zero current. It follows that i_i will have to flow through R_2 to the low-impedance terminal 3. We can then apply Ohm's law to R_2 and determine V_o ; that is,

$$\begin{aligned} V_o &= V_1 - i_i R_2 \\ &= 0 - \frac{V_i}{R_1} R_2 \end{aligned} \quad \dots(10.19)$$

Therefore, the closed-loop voltage gain is

$$A_v = \frac{V_o}{V_i} = -\frac{R_2}{R_1} \quad \dots(10.20)$$

Because of the minus sign associated with closed-loop gain, this configuration is called inverting configuration.

We can also determine the input resistance seen by the voltage source V_i . Due to virtual ground we have, from equation (10.18),

$$i_i = \frac{V_i}{R_1}$$

The input resistance is then defined as

$$R_i = \frac{V_i}{i_i} = R_1$$

This shows that the input resistance seen by the source is a function of R_1 , only, and is a result of the 'virtual ground' concept.

Since there are no coupling capacitors in the op-amp circuit, the input and output voltages, as well as the currents in the resistors, can be dc signals. The inverting op-amp can then amplify dc voltages.